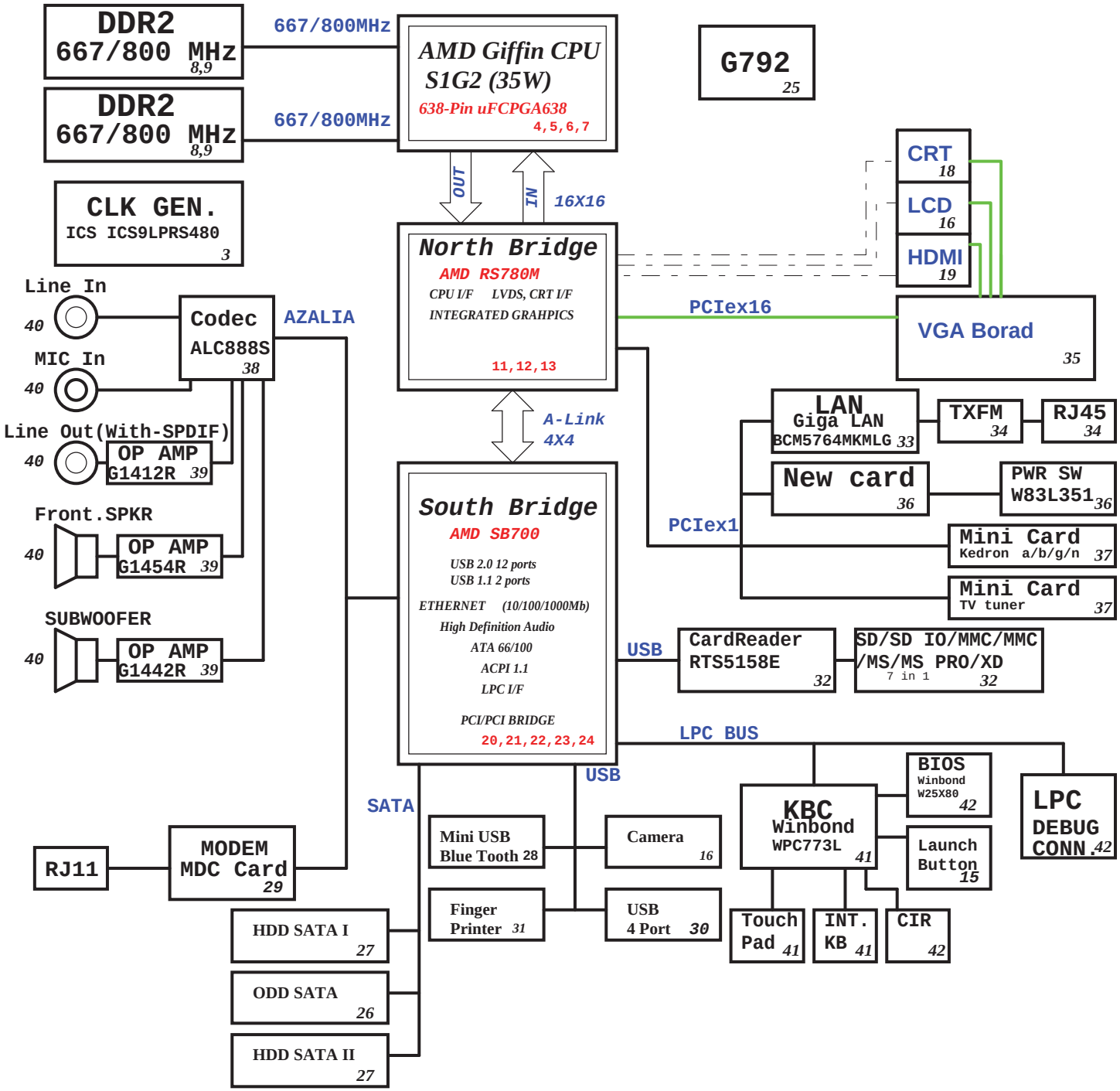
Big Bear 2A (AS 18") Block Diagram

Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 48	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)
RT9026PFP 50	
1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)
RT9166 50	
3D3V_S0	2D5V_S0 (300mA)
G957 50	
3D3V_S0	1D5V_S0(1A)
G9161 50	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731A 51	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Big Bear 2A | Rev: SC

Date: Monday, October 27, 2008 | Sheet 1 of 55

<Core Design>

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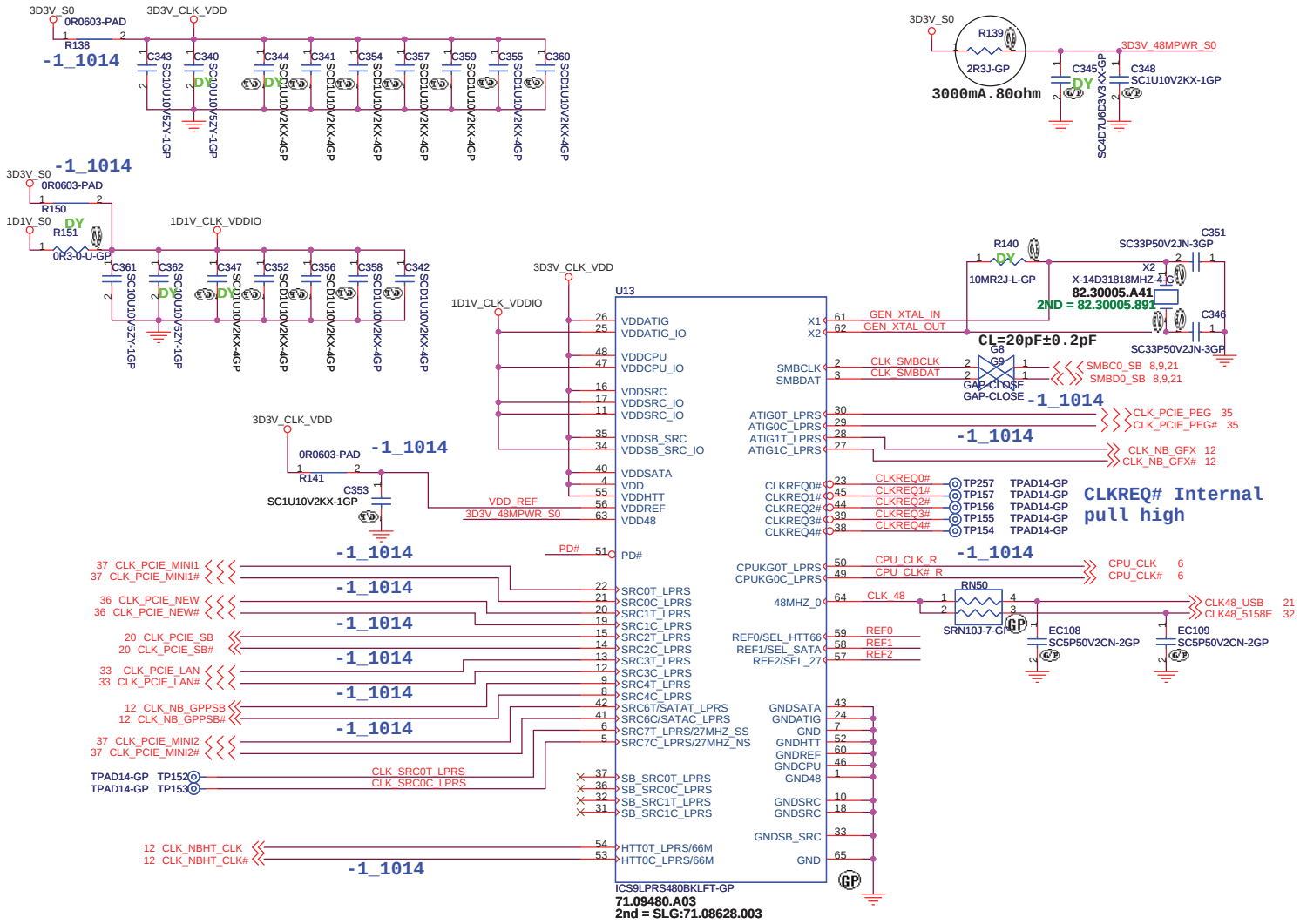
Title		
	HISTORY	
Size	Document Number	Rev
A3	**Big Bear 2A**	**SA**
Date: Monday, October 27, 2008	Sheet 2 of 55	



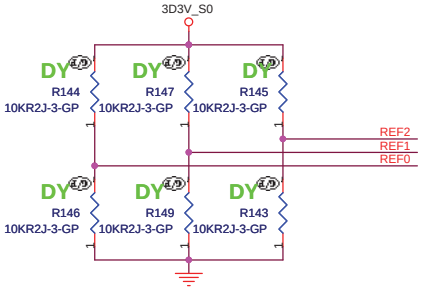
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

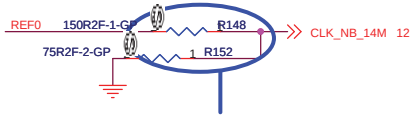
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock

* default

CPU_CLK(200MHz)



	OSC_14M_NB
RS780M	1.1V 158R/90.9R

<Core Design>

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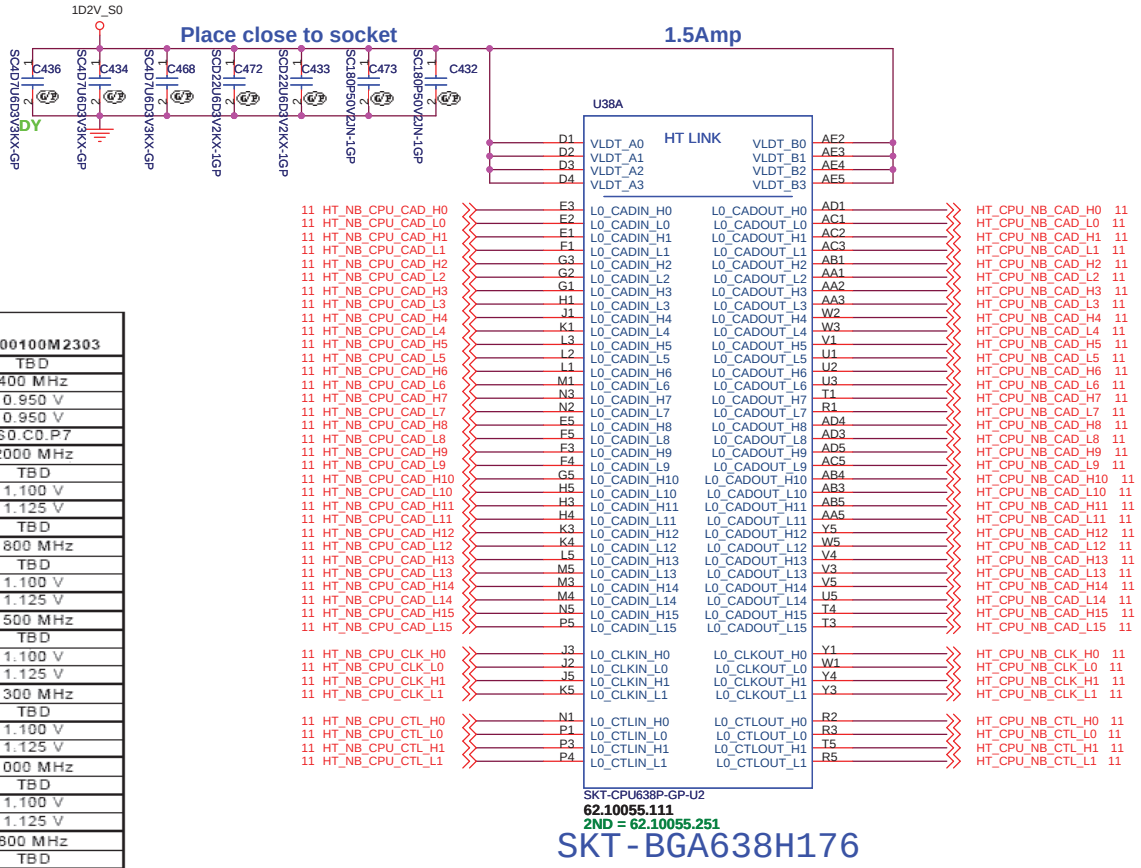
Title: **CLKGEN_ICS9LPRS480**

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 3 of 55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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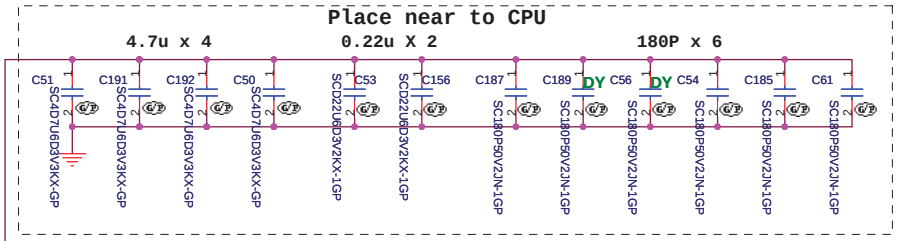
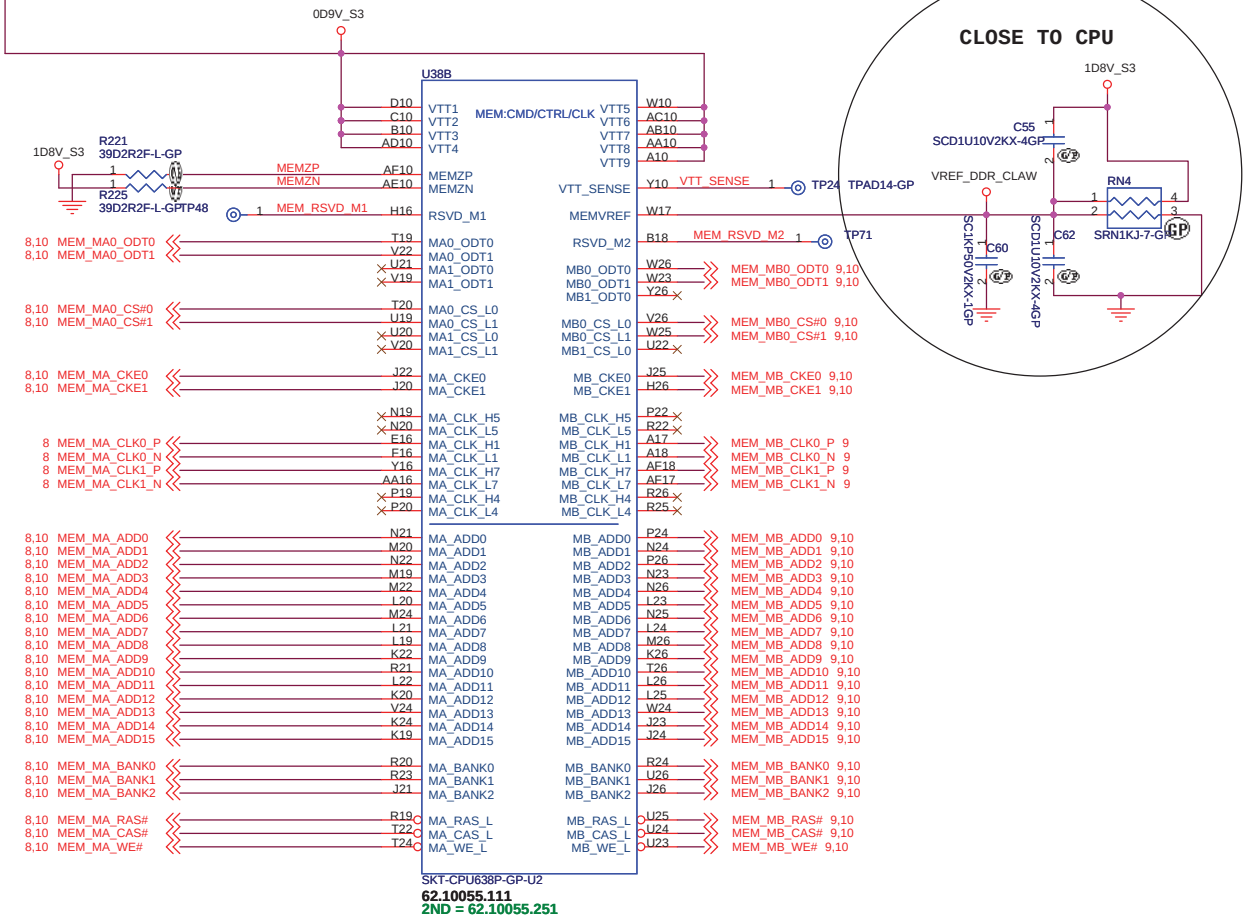
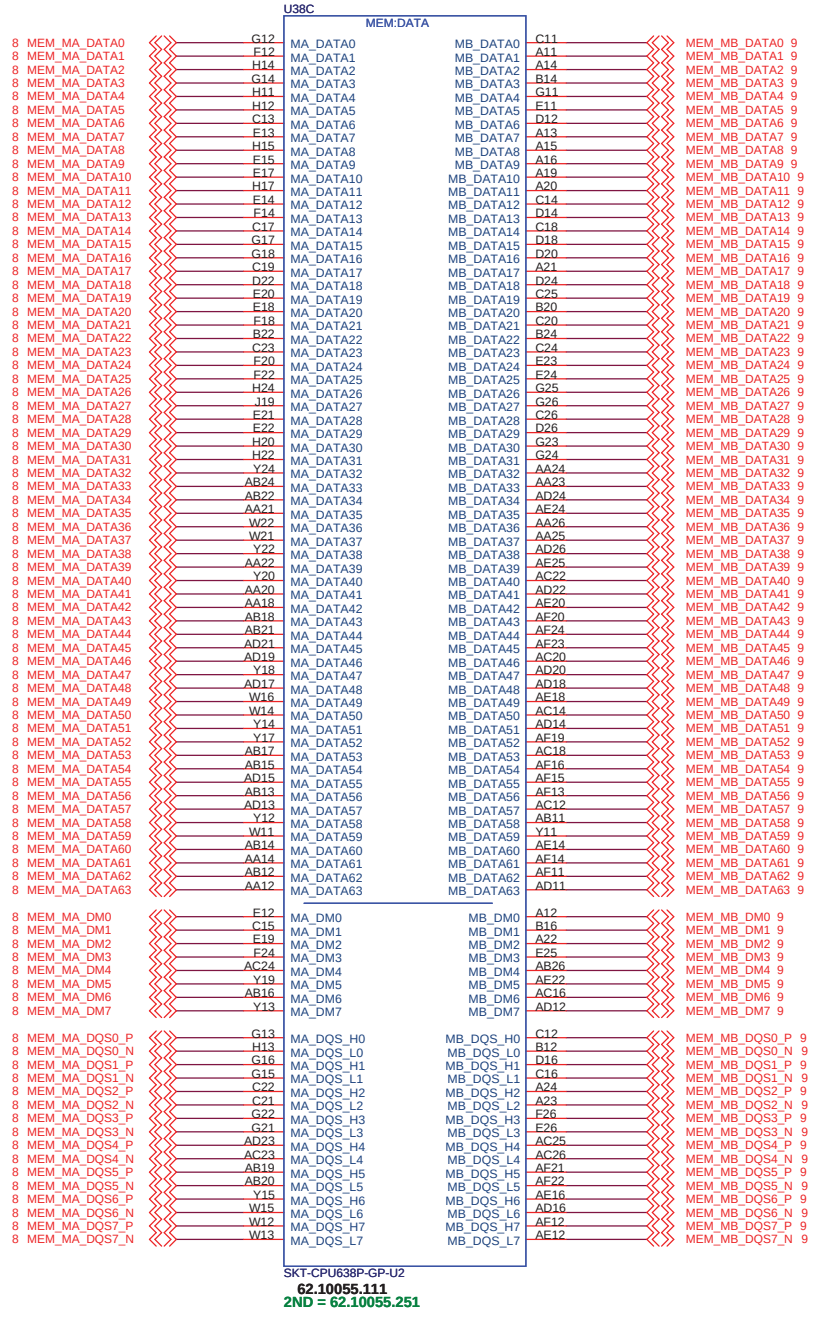
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 4 of 55







<Core Design>

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Title	CPU_DDR_(2/4)
Size	A3
Document Number	Big Bear 2A
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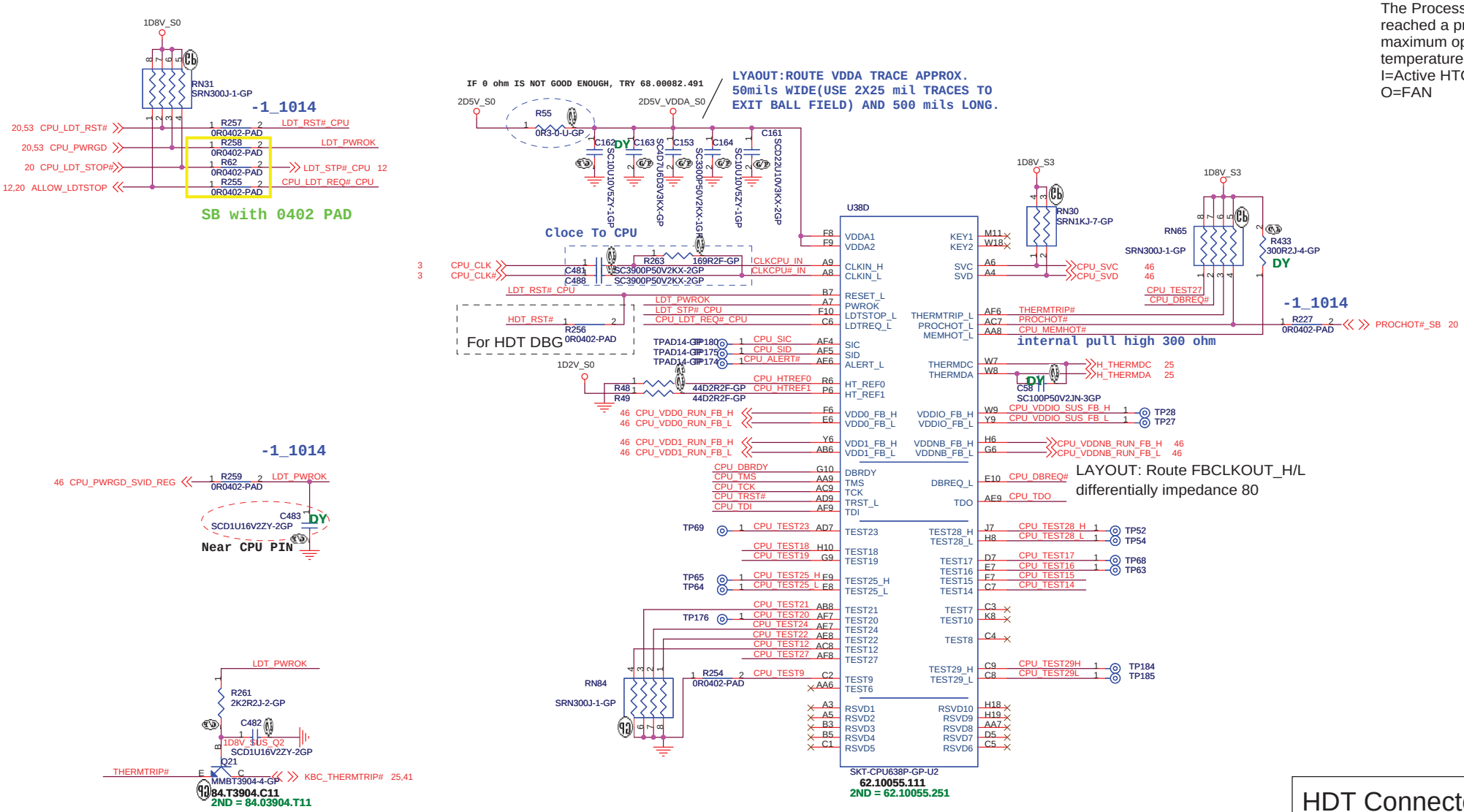
Date:	Monday, October 27, 2008
Sheet	5 of 55

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN



<Core Design>

緯創資通 **Wistron Corporation**
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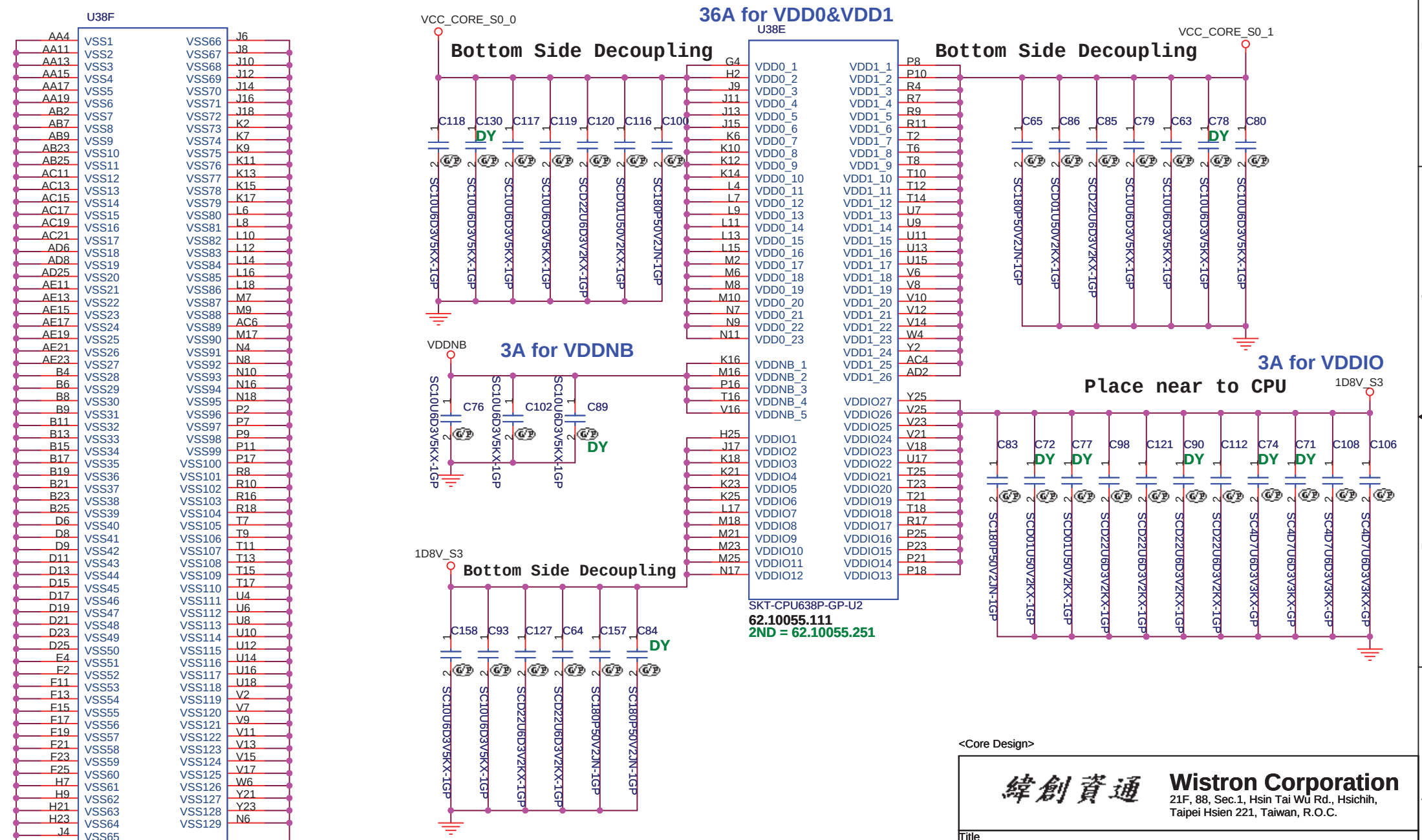
Title: ***CPU_Control&Debug_(3/4)***

Size	Document Number	Rev
A3	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 6 of 55



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
A4	Big Bear 2A	SA

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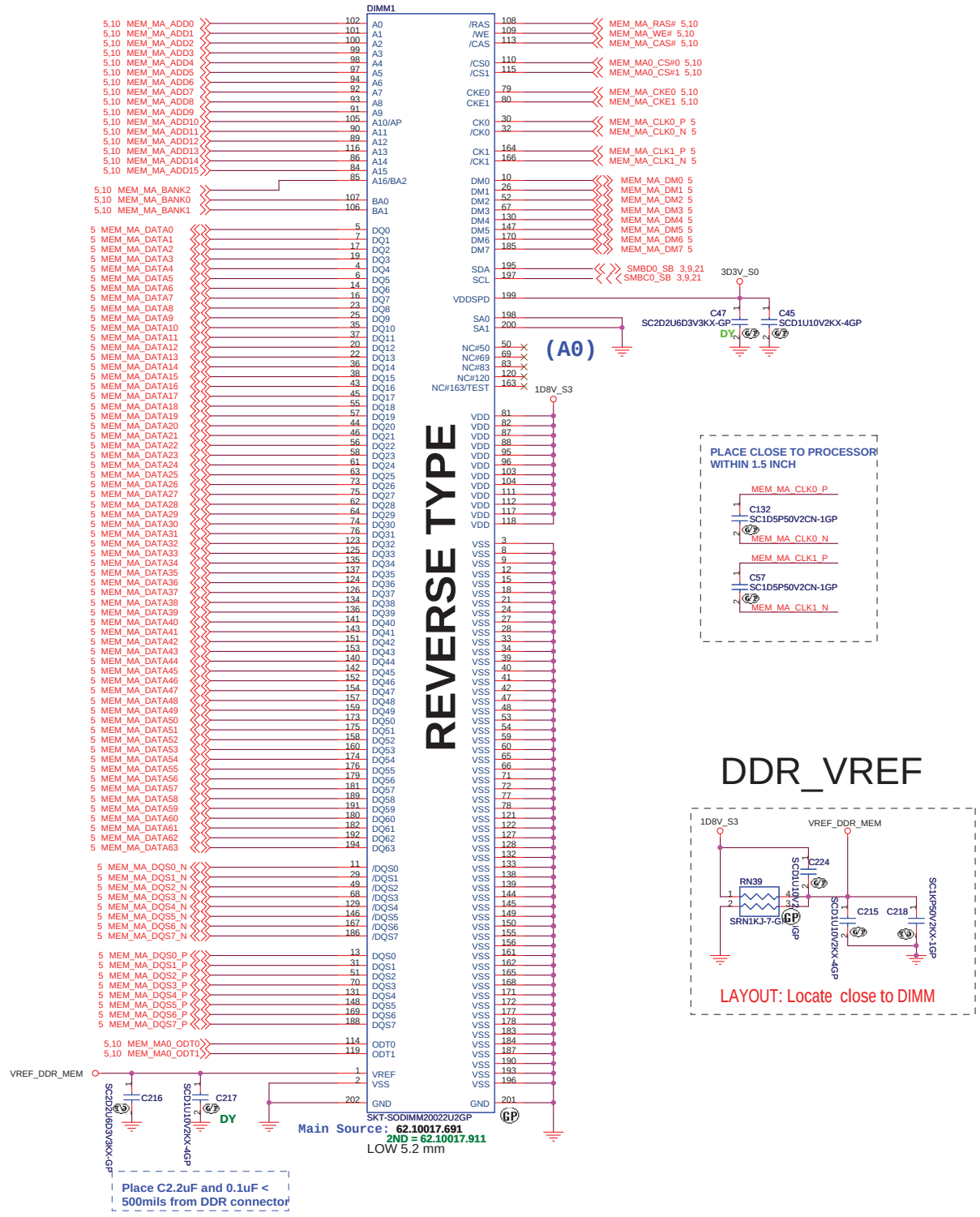
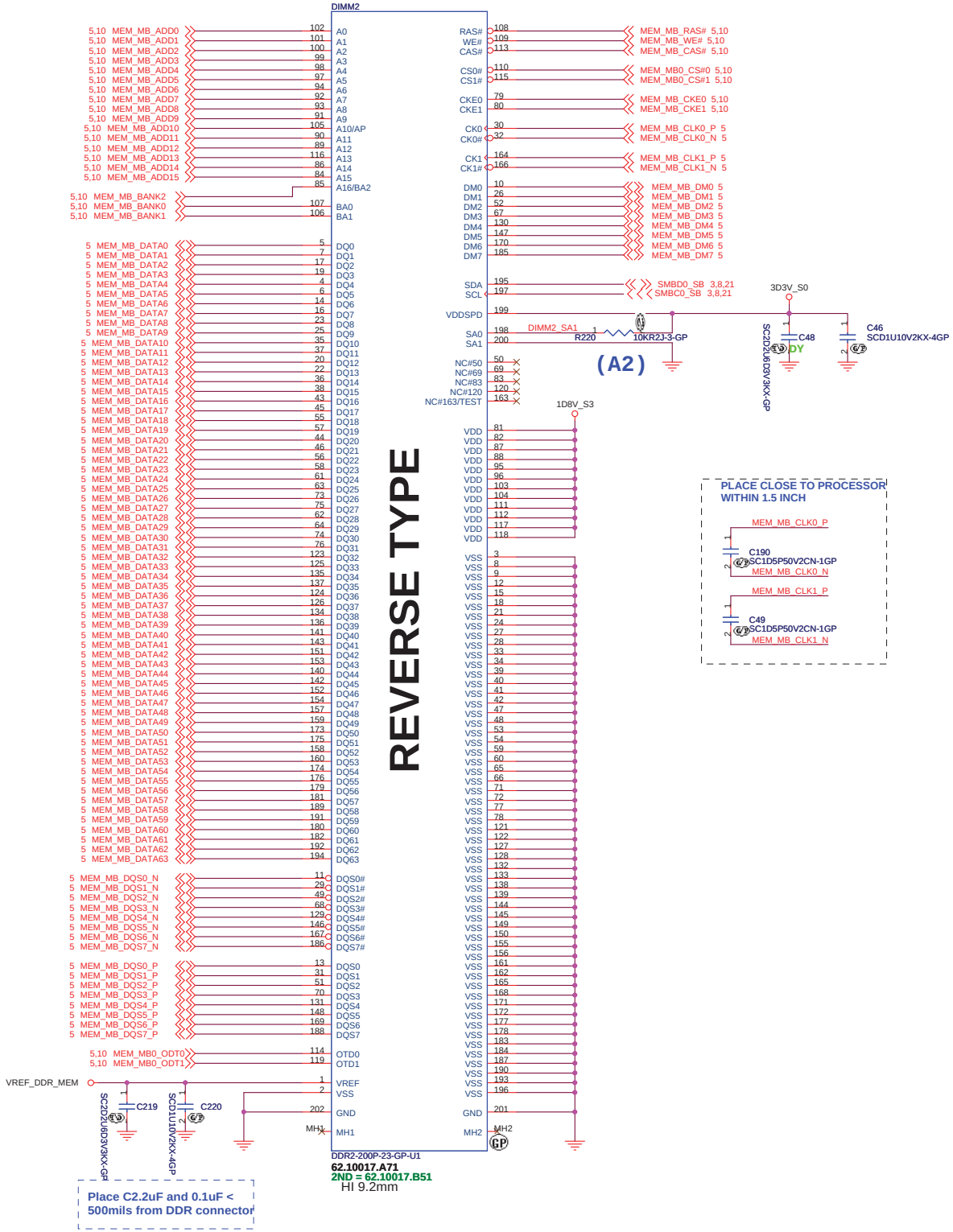


<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR_SO-DIMM SKT_1		
Size Custom	Document Number Big Bear 2A		Rev SA
Date: Monday, October 27, 2008	Sheet 8 of 55		



<Core Design>

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Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Big Bear 2A | Rev: SA

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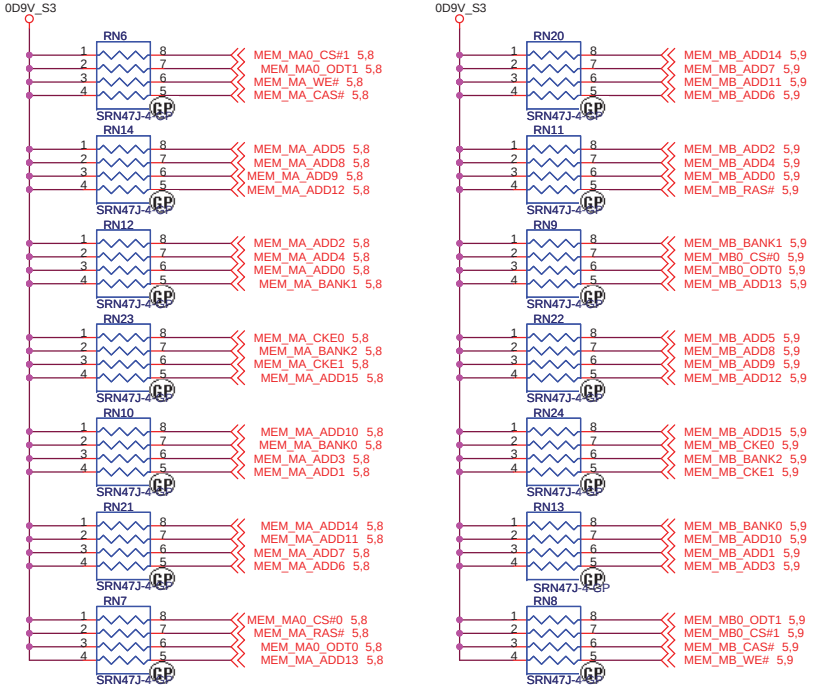
PARALLEL TERMINATION

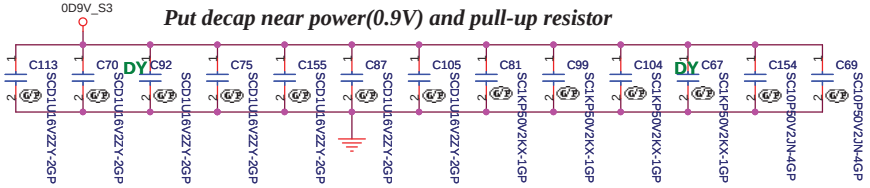
Put decap near power(0.9V) and pull-up resistor



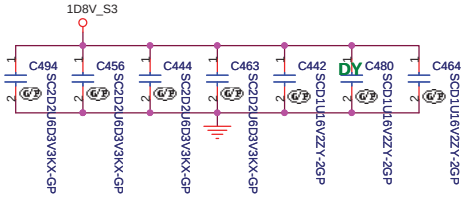
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

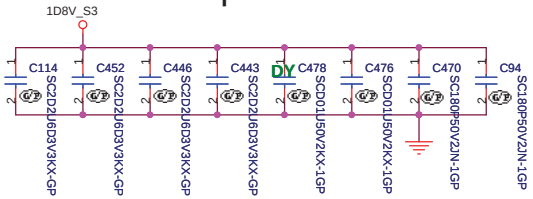


Place these Caps near DM1



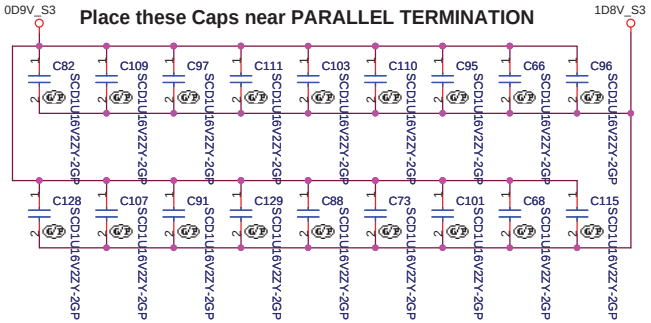
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



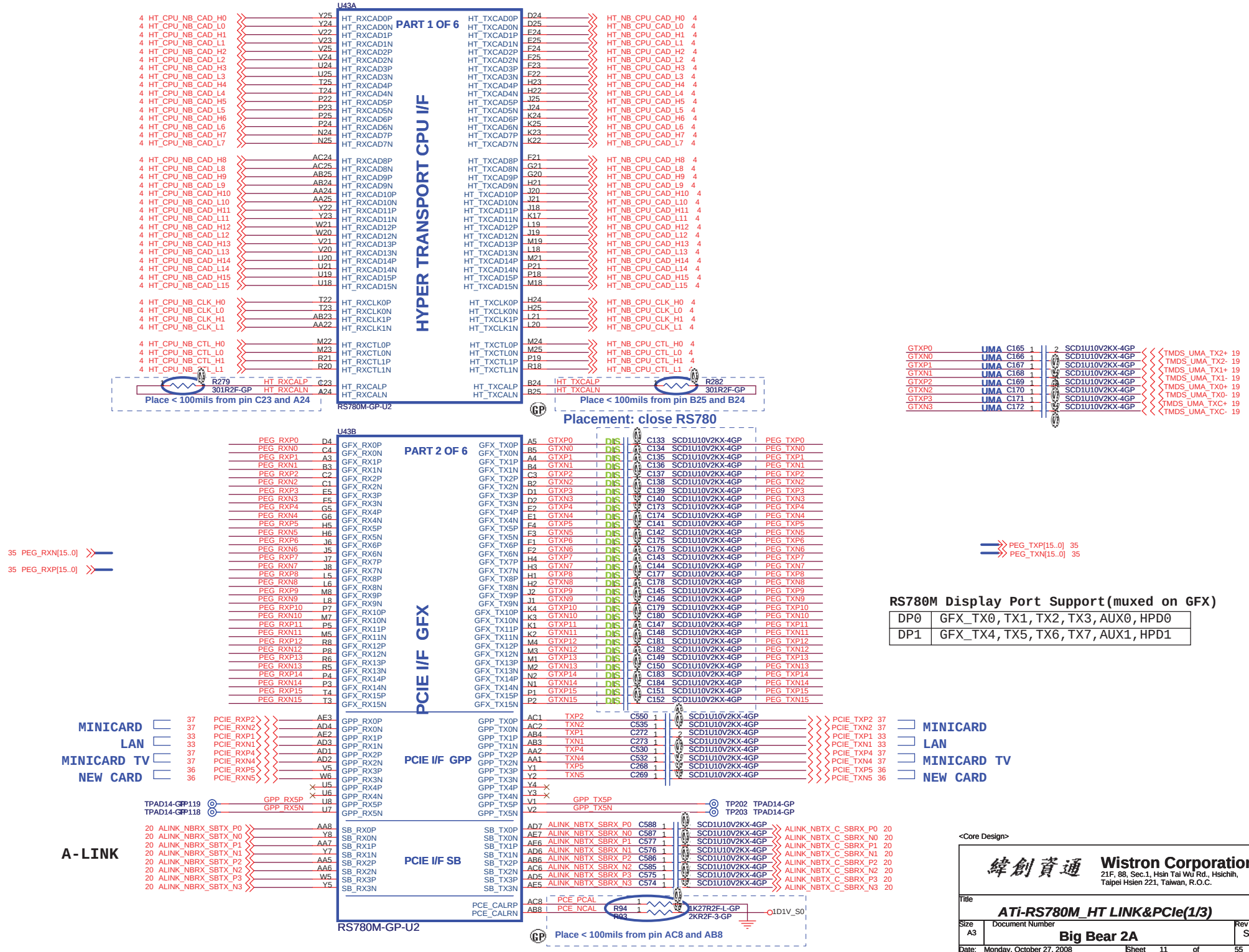
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR_DAMPING & TERMINATION***	
Size A3	Document Number **Big Bear 2A**	Rev SA
Date: Monday, October 27, 2008	Sheet 10 of 55	


U43A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U43B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
MINICARD
LAN
MINICARD TV
NEW CARD
A-LINK
Place < 100mils from pin AC8 and AB8
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number
Big Bear 2A
Rev SA
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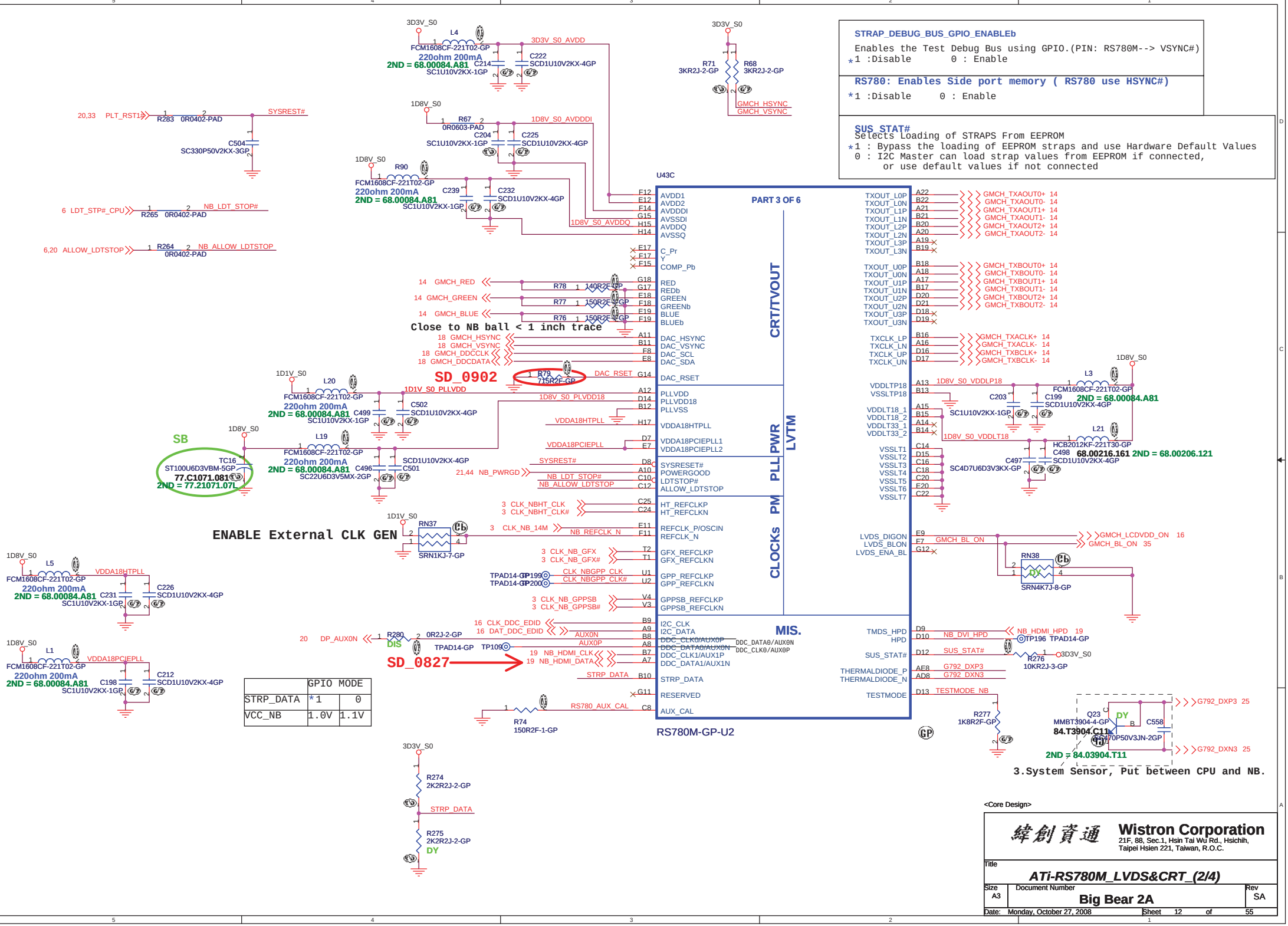
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
Close to NB ball < 1 inch trace
SD_0902
SB
ENABLE External CLK GEN
SD_0827
DIS
3.System Sensor, Put between CPU and NB.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_LVDS&CRT_(2/4)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
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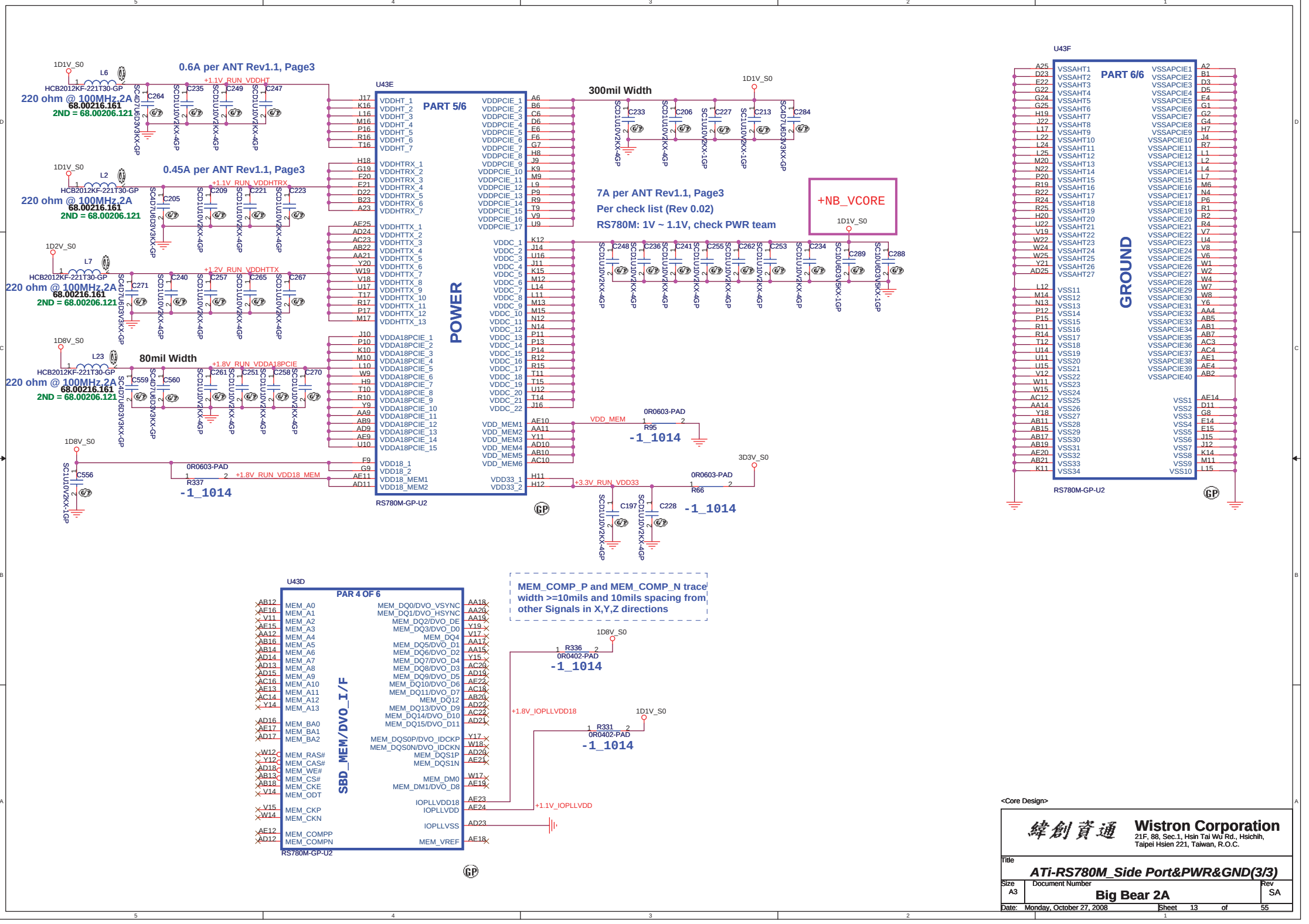

<Core Design>

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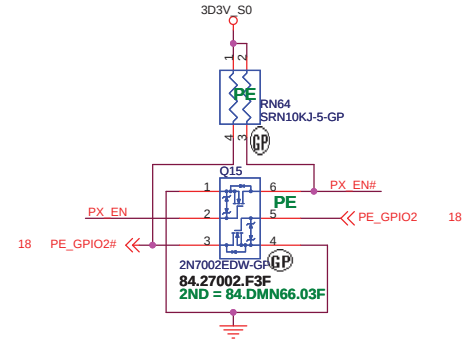
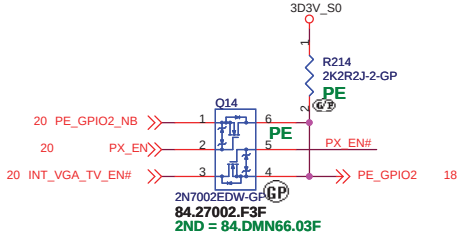
Title: ATi-RS780M_Side Port&PWR&GND(3/3)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

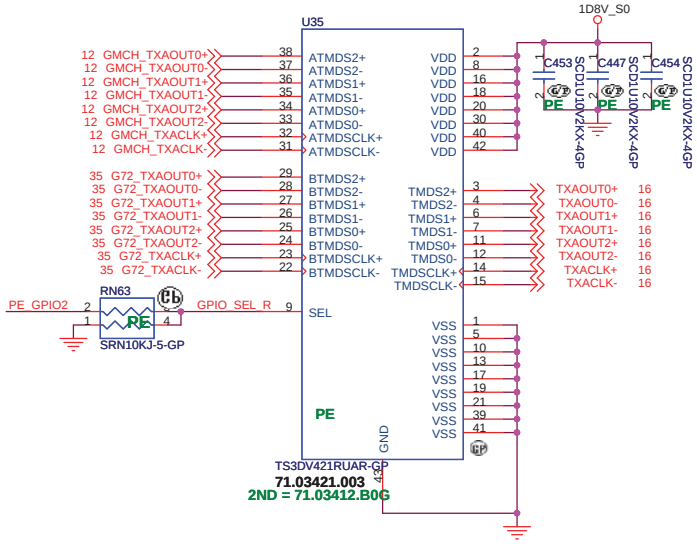
Date: Monday, October 27, 2008 | Sheet 13 of 55

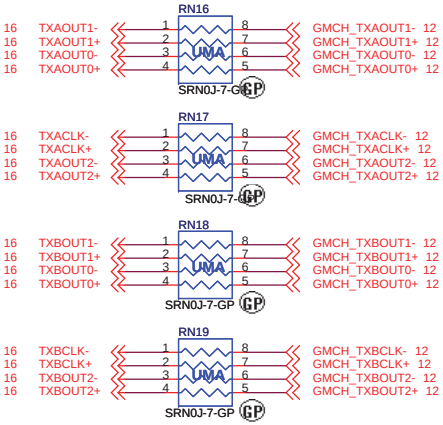


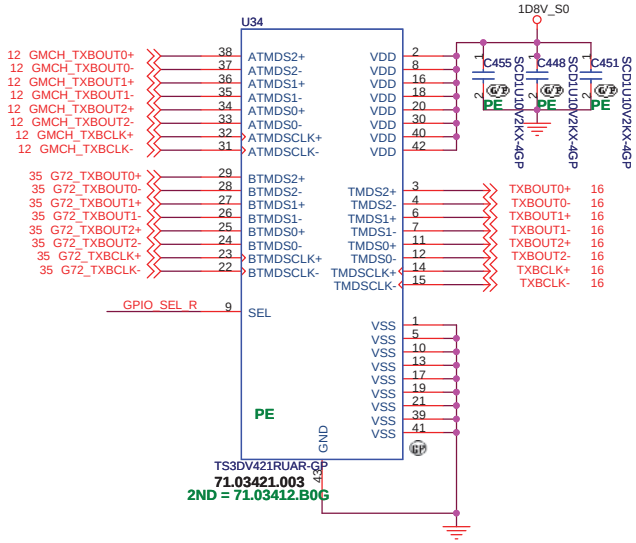


FUNCTION TABLE

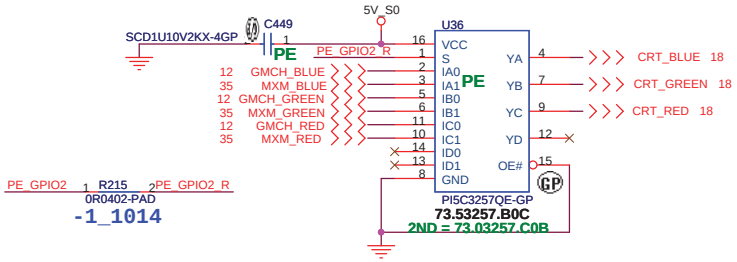
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

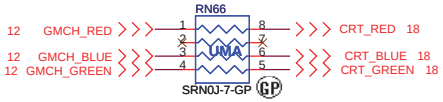






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





<Core Design>

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Title: **SWITCH**

Size: A3 | Document Number: **Big Bear 2A** | Rev: SB

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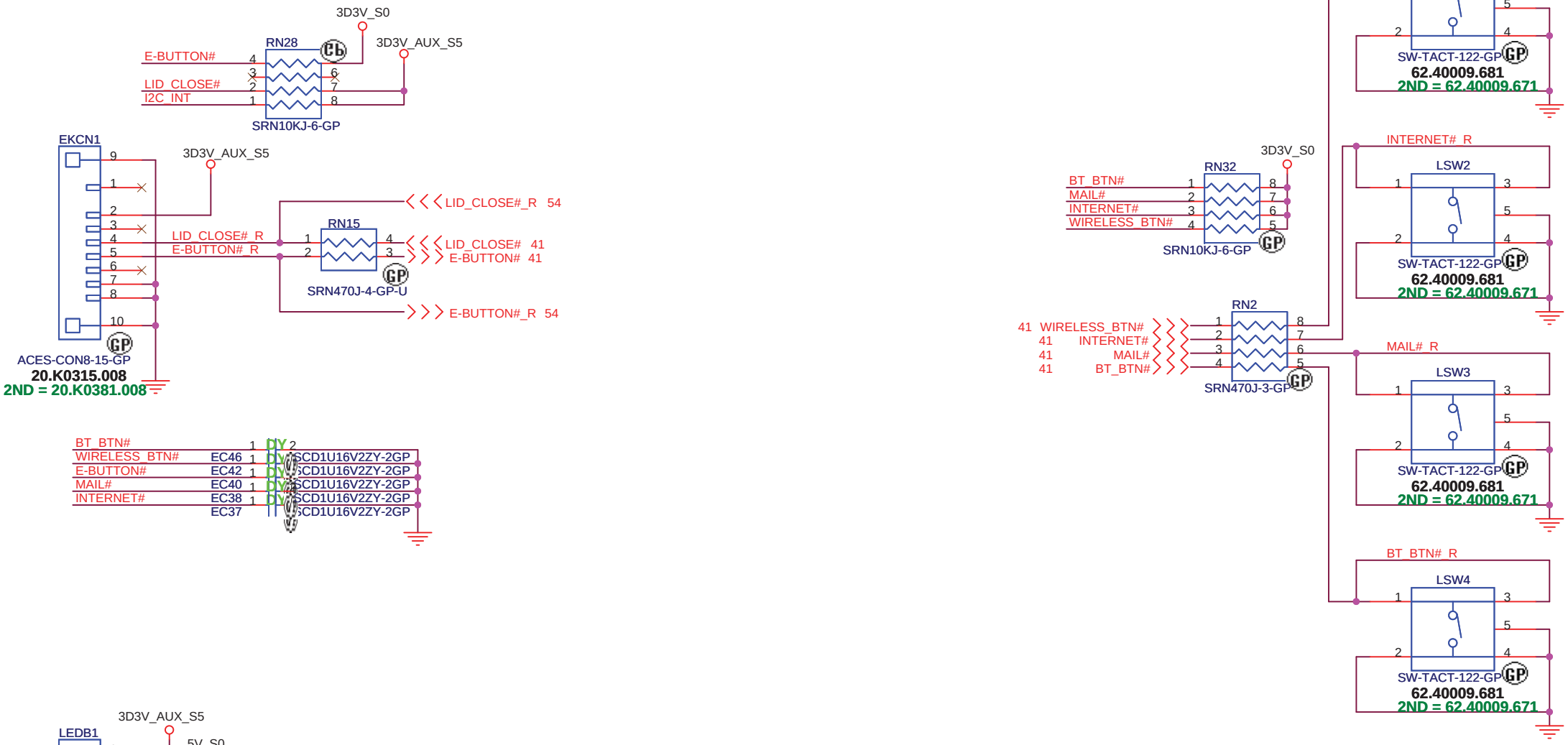
LAUNCH



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LAUNCH & LID***
Size A4	Document Number **Big Bear 2A** Rev SC
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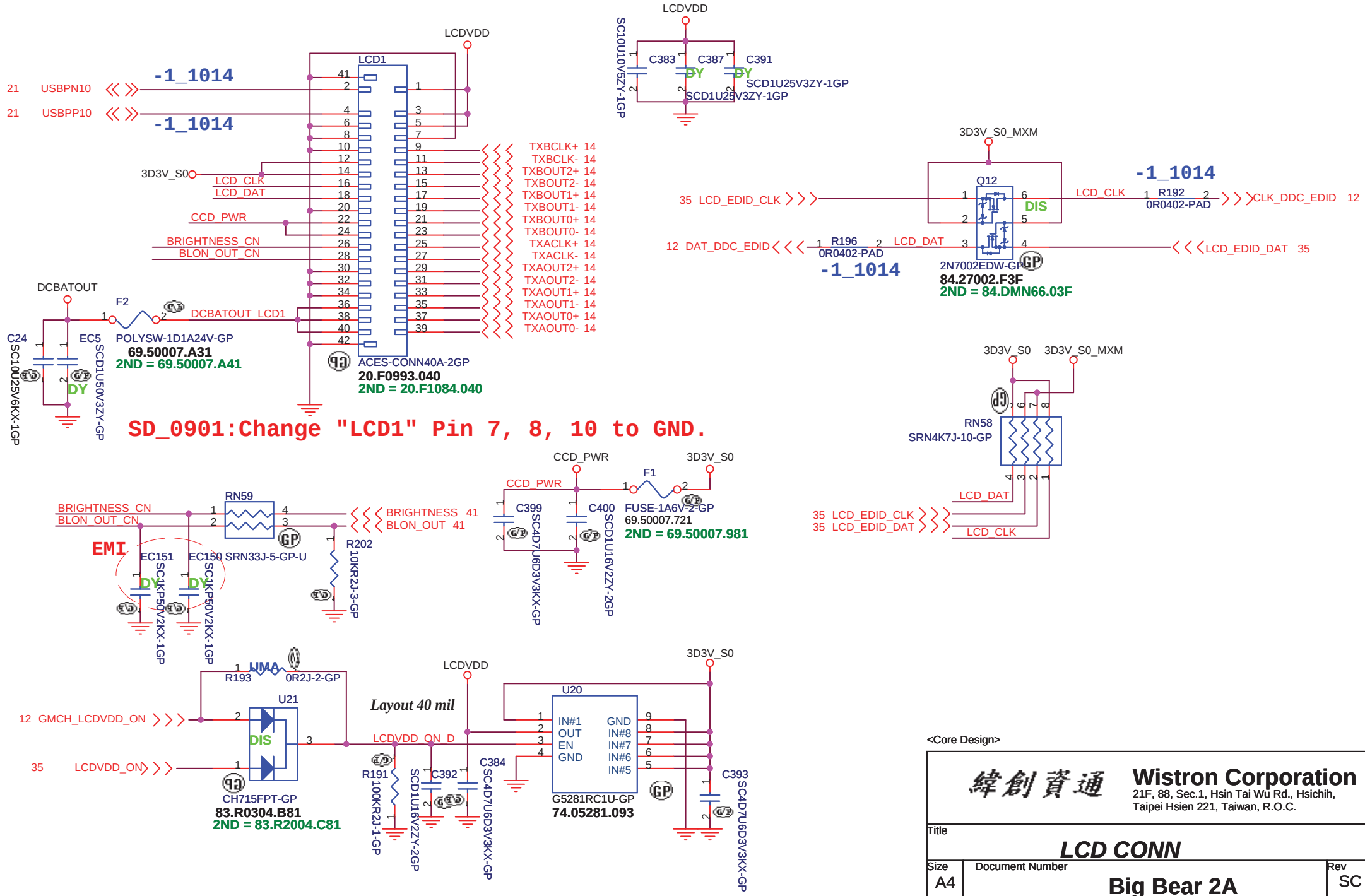
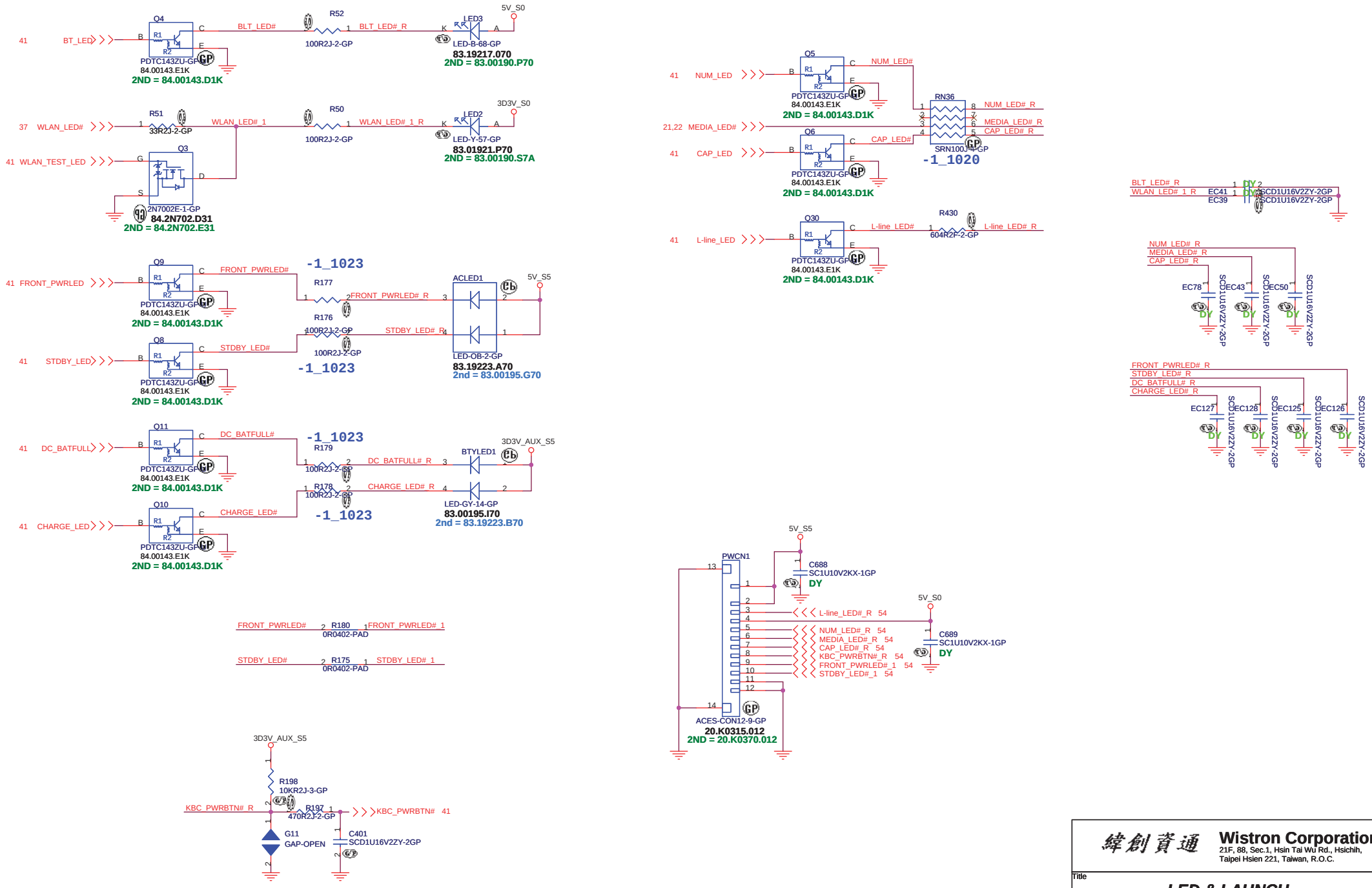
LCD/INVERTER/CCD CONN



<Core Design>

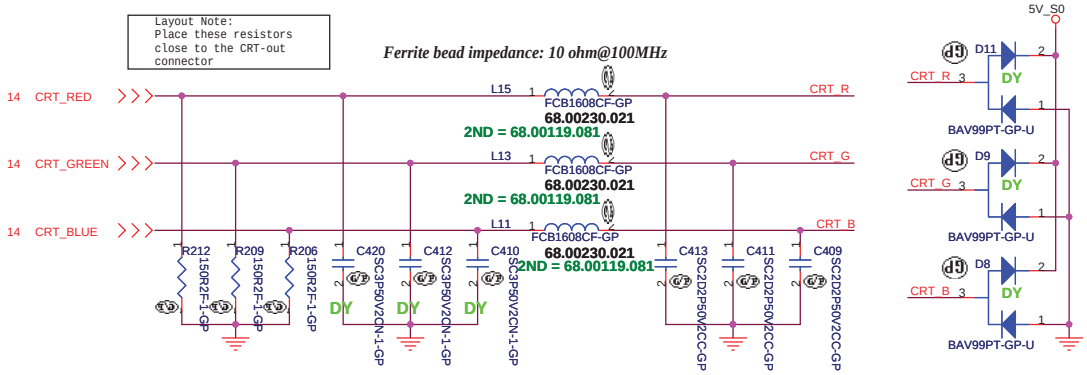
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LCD CONN***	
Size A4	Document Number **Big Bear 2A**	Rev SC
Date: Monday, October 27, 2008	Sheet 16 of 55	

LED



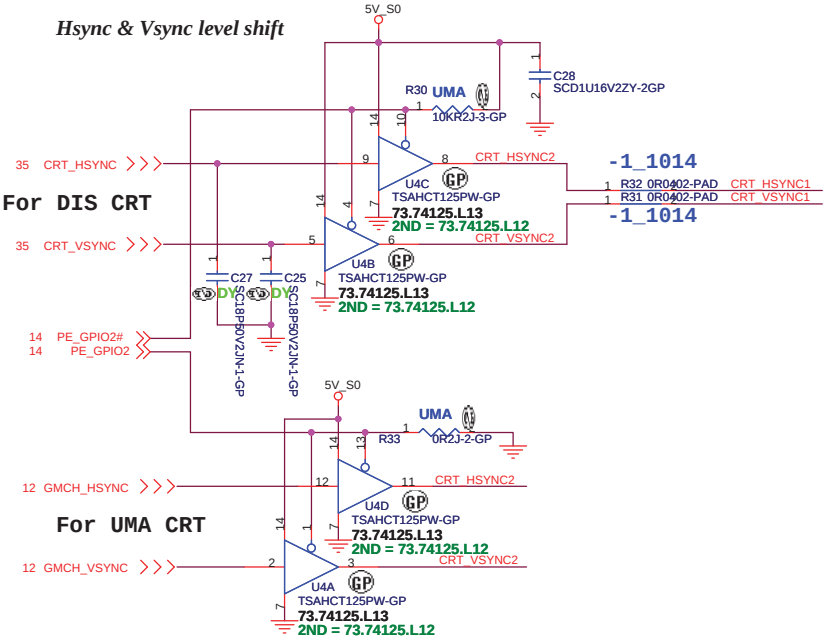
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LED & LAUNCH		
Size: A3	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 17 of 55	

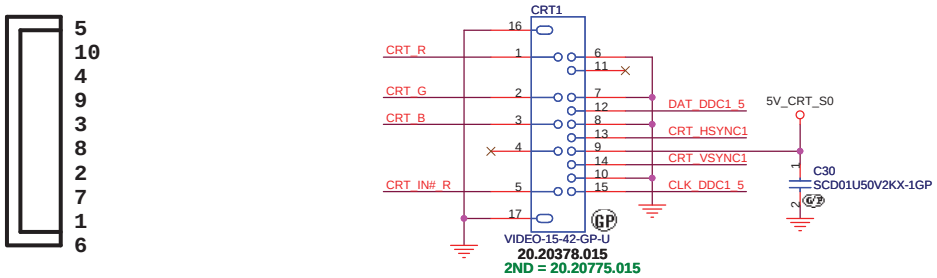


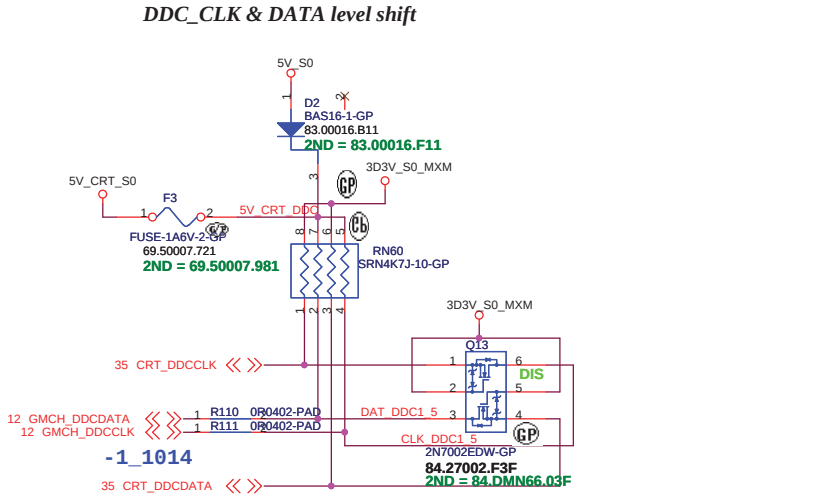
Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR





<Core Design>

緯創資通 **Wistron Corporation**
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Title		
	CRT Connector	
Size	Document Number	Rev
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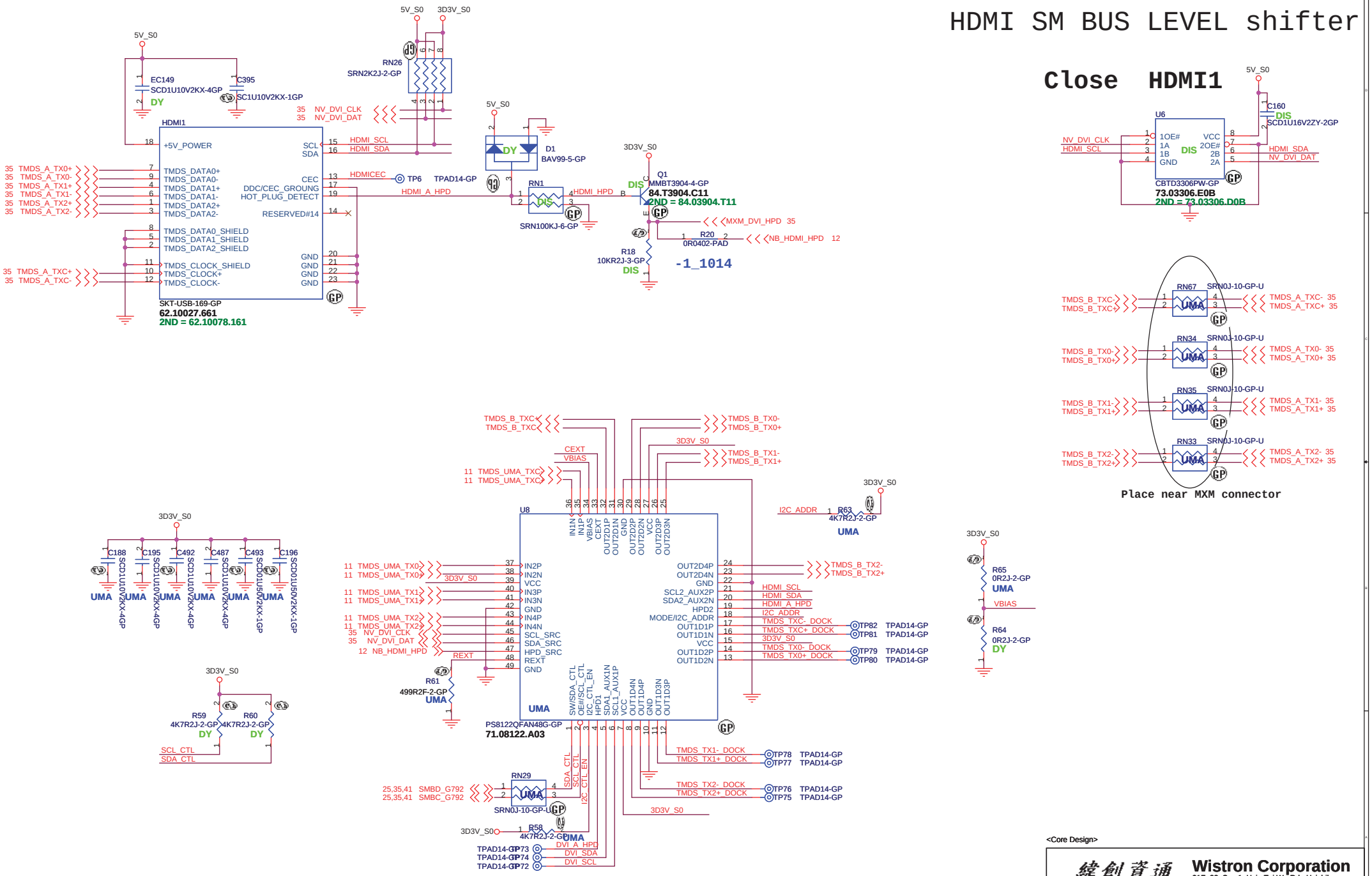
HDMI SM BUS LEVEL shifter



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

Size: A3 | Document Number: Big Bear 2A | Rev: SD

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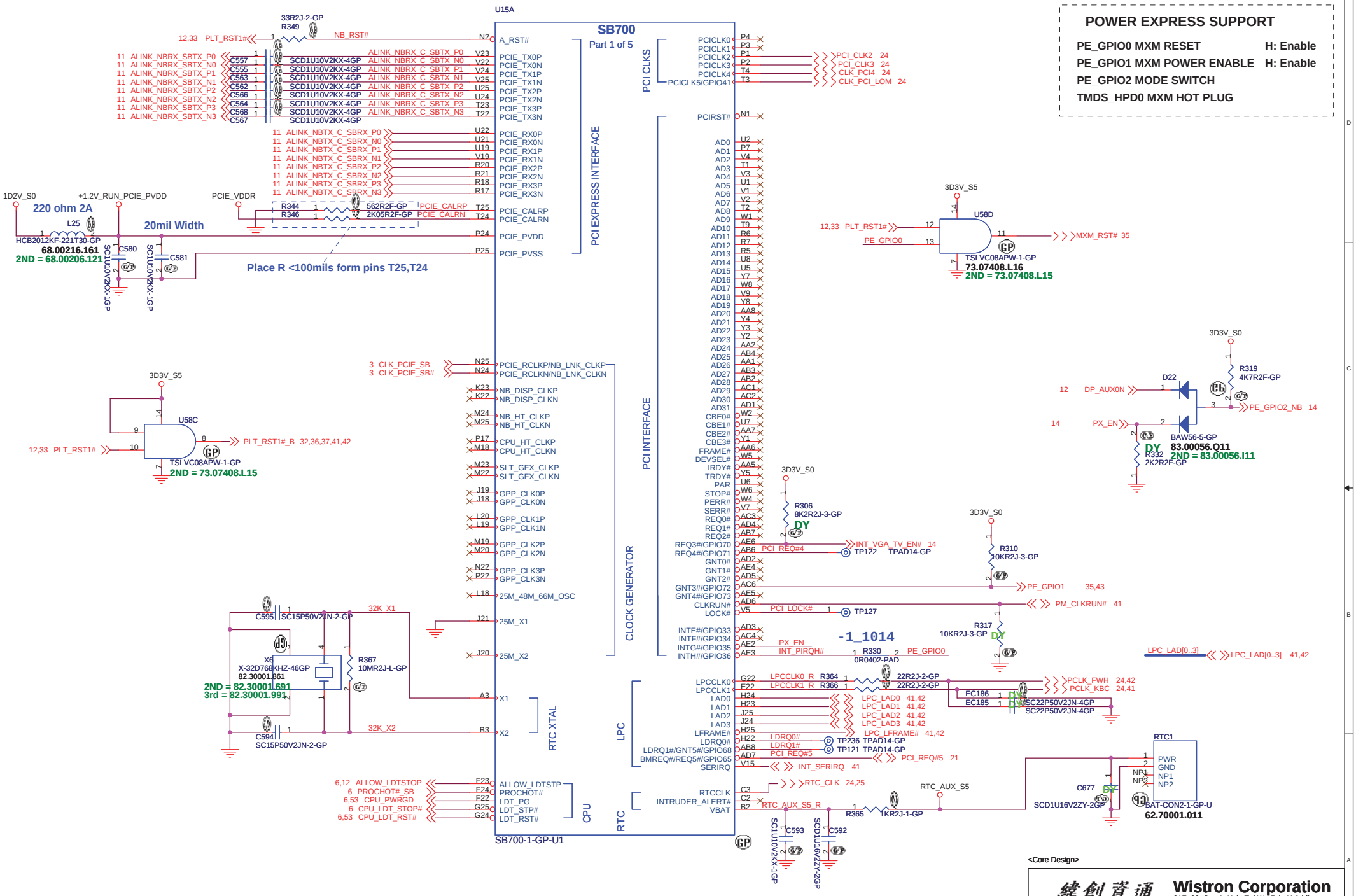
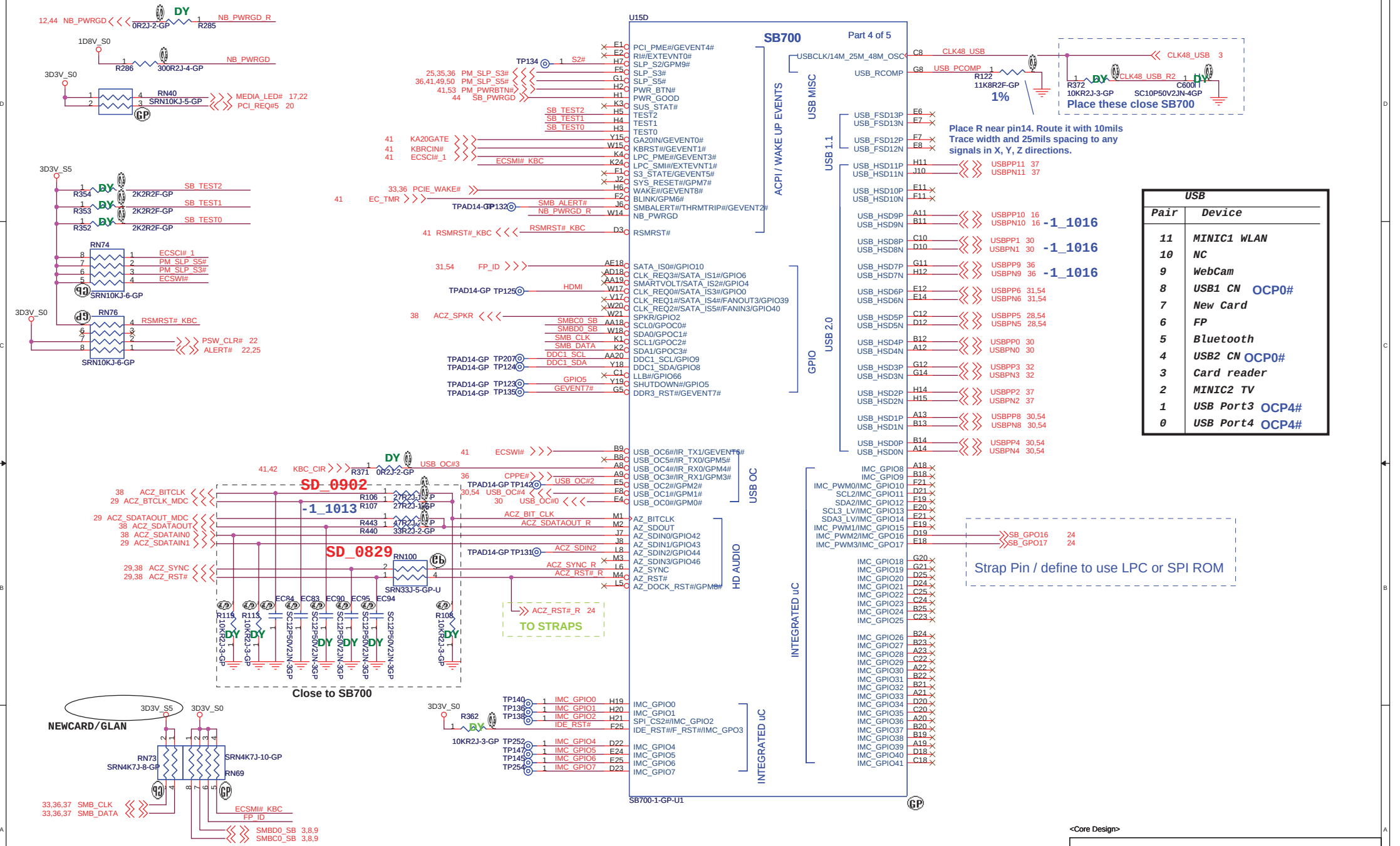

POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
U15A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
LPC
CPU
RTC
SB700-1-GP-U1
33R2J-2-GP
R349
NB_RST#
PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
220 ohm 2A
L25
HCB2012KF-221T30-GP
68.00216.161
2ND = 68.00206.121
20mil Width
C580
C581
SC1U10V2KX-1GP
R344
R346
562R2F-GP
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_PVDD
PCIE_PVSS
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK2 24
PCI_CLK3 24
CLK_PCI4 24
CLK_PCI_LOM 24
PCIRST#
3D3V_S5
U58D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
MXM_RST# 35
3D3V_S0
R319
4K7R2F-GP
D22
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.I11
DP_AUX0N
PE_GPIO2_NB 14
PX_EN
R332
2K2R2F-GP
U58C
PLT_RST1#_B 32,36,37,41,42
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
32K_X1
32K_X2
C595
SC15P50V2JN-2-GP
X6
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
3rd = 82.30001.991
R367
10MR2J-L-GP
C594
SC15P50V2JN-2-GP
ALLOW_LDTSTOP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
LDT_PG
LDT_STP#
LDT_RST#
REQ3#/GPIO70
REQ4#/GPIO71
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
R306
8K2R2J-3-GP
DY
INT_VGA_TV_EN# 14
PCI_REQ#4
TP122
TPAD14-GP
R310
10KR2J-3-GP
PE_GPIO1 35,43
PM_CLKRUN# 41
PCI_LOCK#
TP127
R317
10KR2J-3-GP
-1_1014
PX_EN
INT_PIRQH#
R330
0R0402-PAD
PE_GPIO0
LPC_LAD[0..3]
LPC_LAD[0..3] 41,42
LPCCLK0
LPCCLK1
LPCCLK0_R R364
LPCCLK1_R R366
22R2J-2-GP
PCLK_FWH 24,42
PCLK_KBC 24,41
EC186
EC185
SC22P50V2JN-4GP
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPC_LAD0 41,42
LPC_LAD1 41,42
LPC_LAD2 41,42
LPC_LAD3 41,42
LPC_LFRAME# 41,42
LDRQ0#
TP236
TPAD14-GP
LDRQ1#
TP121
TPAD14-GP
PCI_REQ#5
PCI_REQ#5 21
INT_SERIRQ 41
RTC_CLK 24,25
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_AUX_S5_R
R365
1KR2J-1-GP
RTC_AUX_S5
C593
C592
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
RTC1
PWR
GND
NP1
NP2
C677
SCD1U16V2ZY-2GP
BAT-CON2-1-GP-U
62.70001.011
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 20 of 55



USB	
Pair	Device
11	MINIC1 WLAN
10	NC
9	WebCam
8	USB1 CN OCP0#
7	New Card
6	FP
5	Bluetooth
4	USB2 CN OCP0#
3	Card reader
2	MINIC2 TV
1	USB Port3 OCP4#
0	USB Port4 OCP4#

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB700_USB&GPIO_(2/5)**

Size: A3 | Document Number: **Big Bear 2A** | Rev: SA

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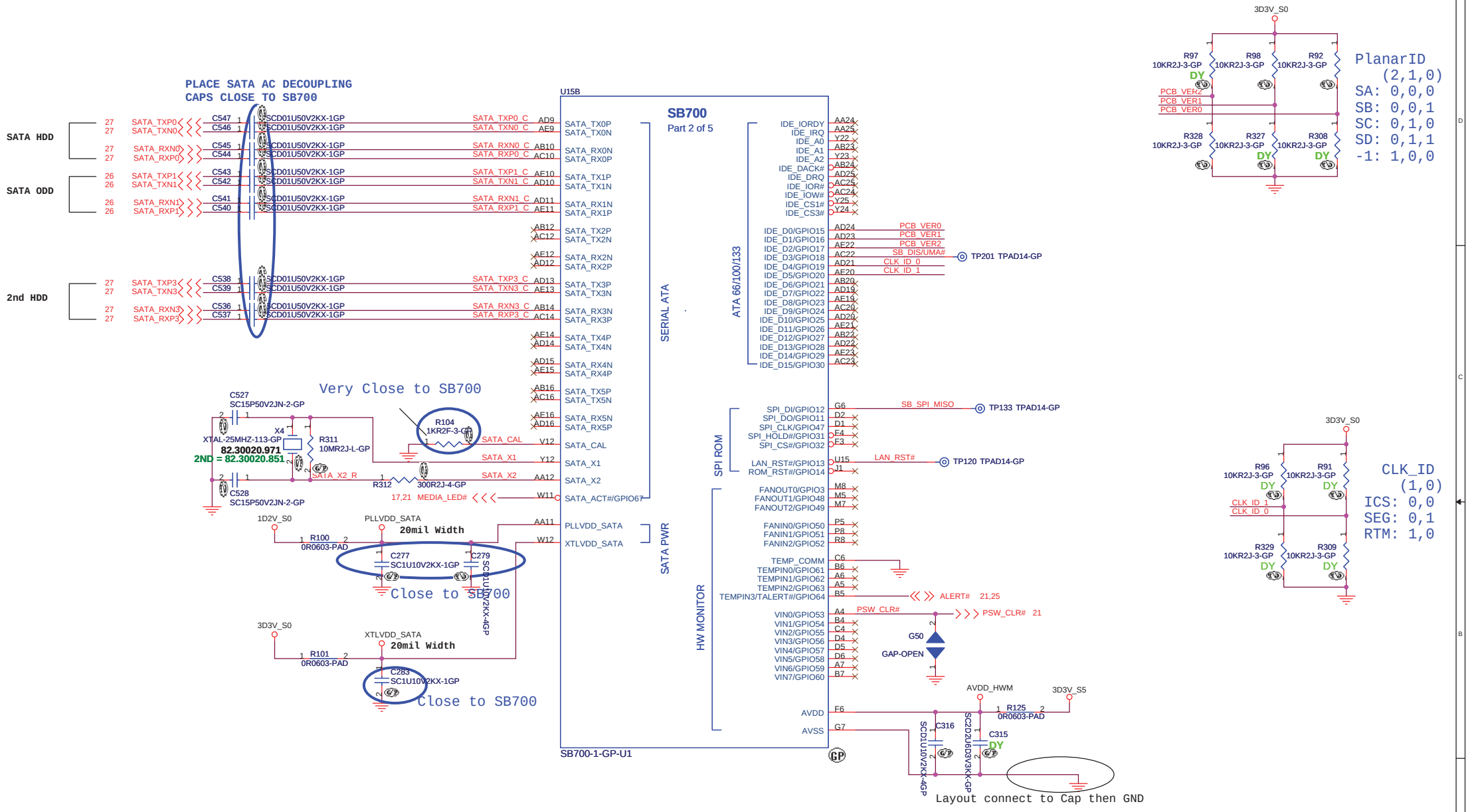
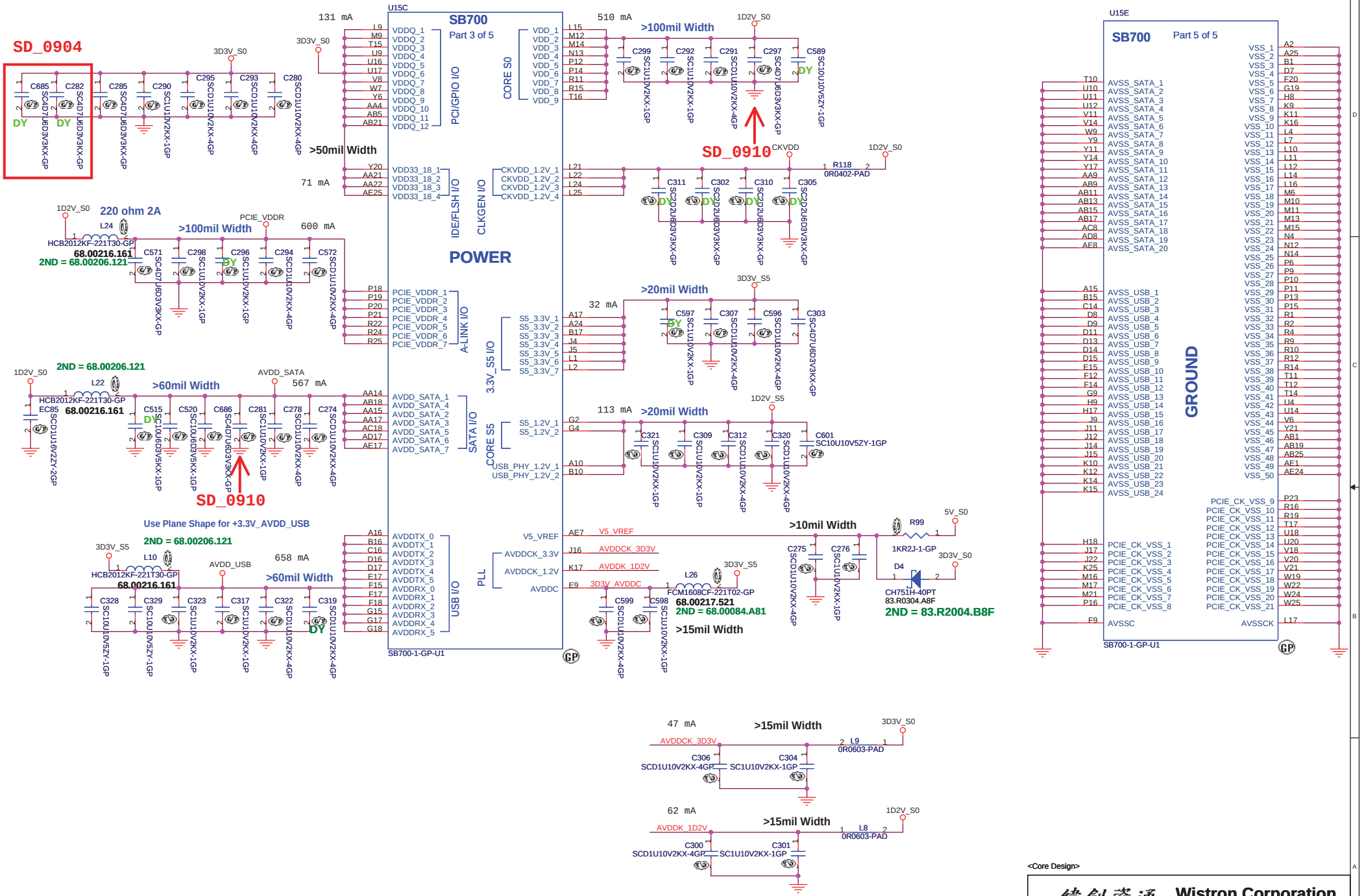


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SB

Date: Monday, October 27, 2008 | Sheet 22 of 55



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_POWER&GND_(4/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

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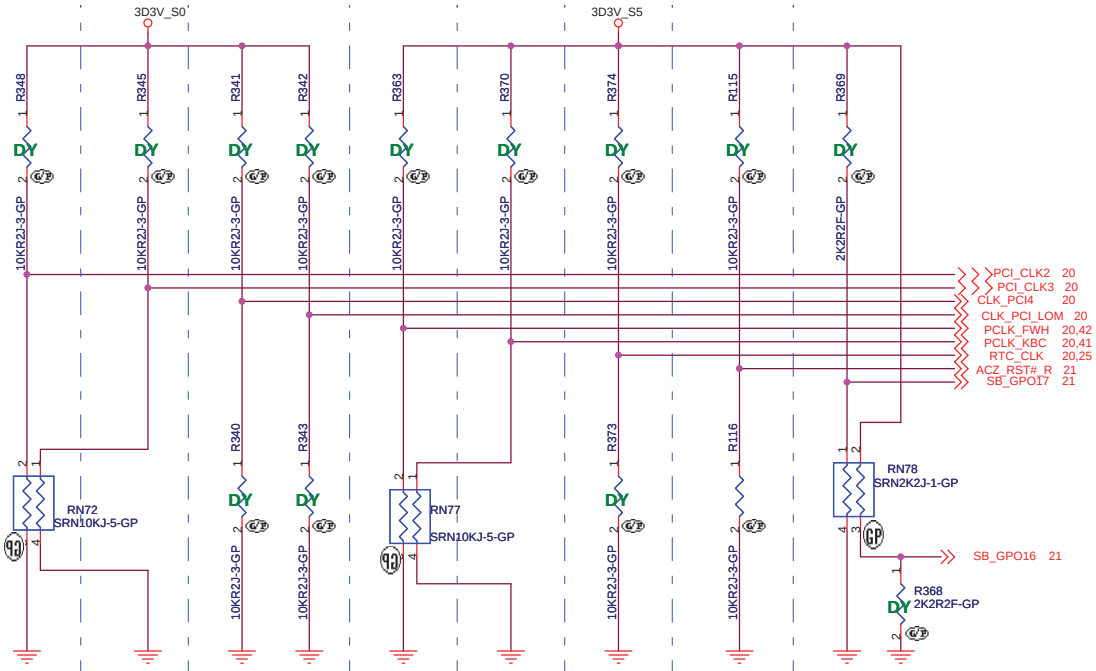
REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATi-SB700_STRAPPING_(5/5)***

Size: A3 | Document Number: **Big Bear 2A** | Rev: SA

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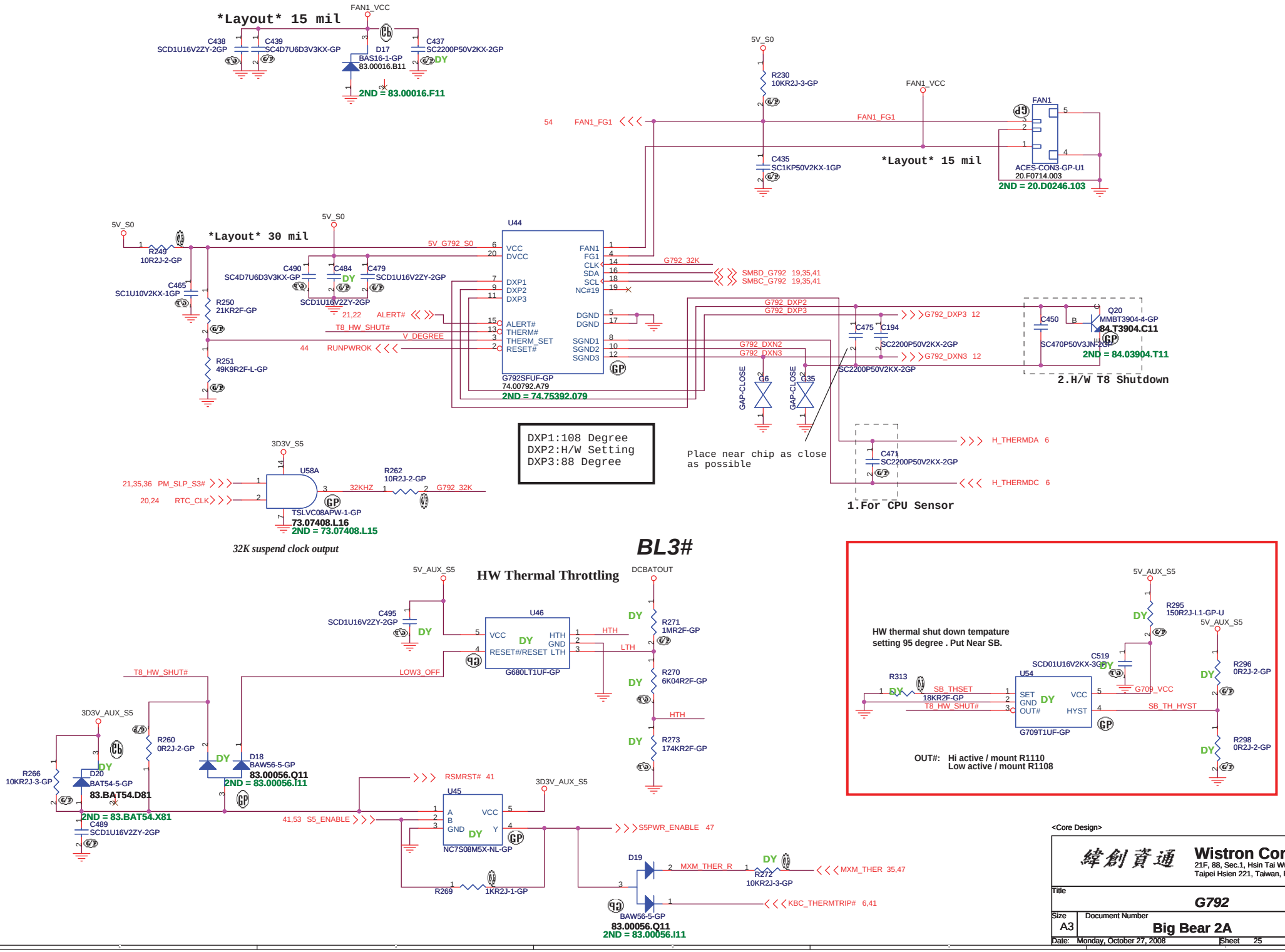
Layout 15 mil
FAN1_VCC
C438 SCD1U16V2ZY-2GP
C439 SC4D7U6D3V3KX-GP
D17 BAS16-1-GP 83.00016.B11
C437 SC2200P50V2KX-2GP
2ND = 83.00016.F11
5V_S0
R230 10KR2J-3-GP
FAN1_VCC
FAN1
54 FAN1_FG1
FAN1_FG1
C435 SC1KP50V2KX-1GP
Layout 15 mil
ACES-CON3-GP-U1 20.F0714.003
2ND = 20.D0246.103
5V_S0
R249 10R2J-2-GP
Layout 30 mil
5V_S0
5V_G792_S0
U44
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792_32K
SMBD_G792 19,35,41
SMBC_G792 19,35,41
C465 SC1U10V2KX-1GP
R250 21KR2F-GP
C490 SC4D7U6D3V3KX-GP
C484
C479 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
21,22 ALERT#
T8_HW_SHUT#
V_DEGREE
44 RUNPWROK
R251 49K9R2F-L-GP
G792SFUF-GP 74.00792.A79
2ND = 74.75392.079
G792_DXP2
G792_DXP3
G792_DXP3 12
C475
C194
SC2200P50V2KX-2GP
G792_DXN2
G792_DXN3
G792_DXN3 12
SC2200P50V2KX-2GP
GAP-CLOSE
G6
GAP-CLOSE
G35
C450
Q20 MMBT3904-4-GP 84.T3904.C11
SC470P50V3JN-2GP
2ND = 84.03904.T11
2.H/W T8 Shutdown
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C471 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
U58A
21,35,36 PM_SLP_S3#
20,24 RTC_CLK
32KHZ
R262 10R2J-2-GP
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
32K suspend clock output
BL3#
HW Thermal Throttling
5V_AUX_S5
DCBATOUT
C495 SCD1U16V2ZY-2GP
U46
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1UF-GP
R271 1MR2F-GP
R270 6K04R2F-GP
R273 174KR2F-GP
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R260 0R2J-2-GP
D18 BAW56-5-GP 83.00056.Q11
2ND = 83.00056.I11
R266 10KR2J-3-GP
D20 BAT54-5-GP 83.BAT54.D81
2ND = 83.BAT54.X81
C489 SCD1U16V2ZY-2GP
RSMRST# 41
U45
A
B
GND
VCC
Y
NC7S08M5X-NL-GP
41,53 S5_ENABLE
3D3V_AUX_S5
S5PWR_ENABLE 47
R269 1KR2J-1GP
D19
MXM_THER_R
R272 10KR2J-3-GP
MXM_THER 35,47
BAW56-5-GP 83.00056.Q11 2ND = 83.00056.I11
KBC_THERMTRIP# 6,41
HW thermal shut down tempature setting 95 degree . Put Near SB.
5V_AUX_S5
R295 150R2J-L1-GP-U
5V_AUX_S5
R313 18KR2F-GP
SB_THSET
T8_HW_SHUT#
SCD01U16V2KX-3GP
C519
U54
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
G709_VCC
SB_TH_HYST
R296 0R2J-2-GP
R298 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
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Document Number
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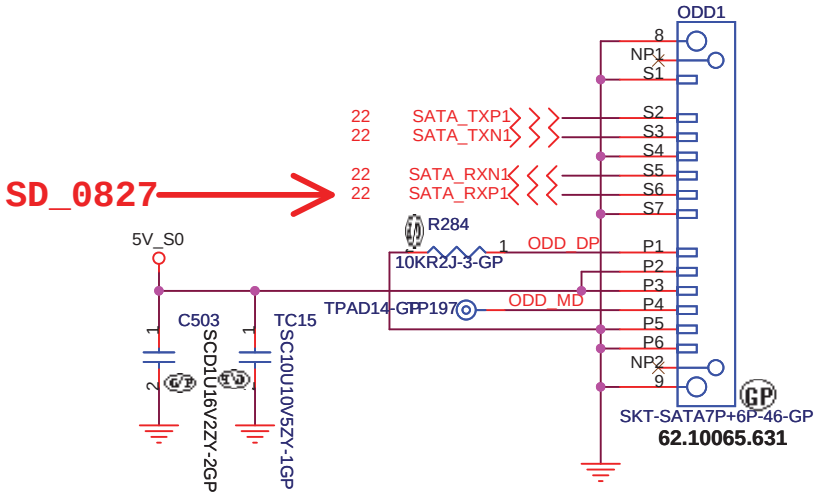
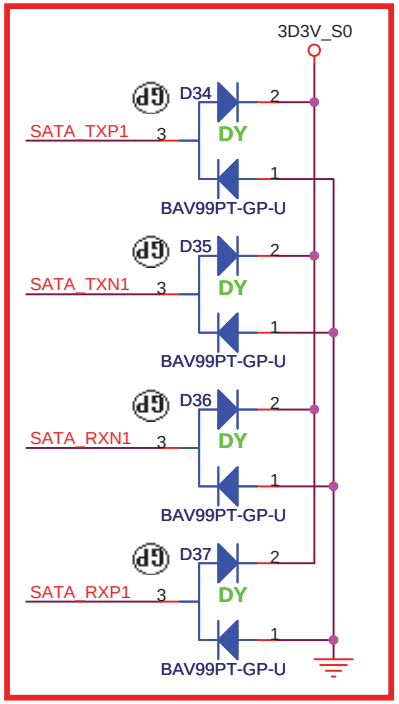
ODD Connector



SD_0828



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CDROM		
Size: A4	Document Number: Big Bear 2A	Rev: SD
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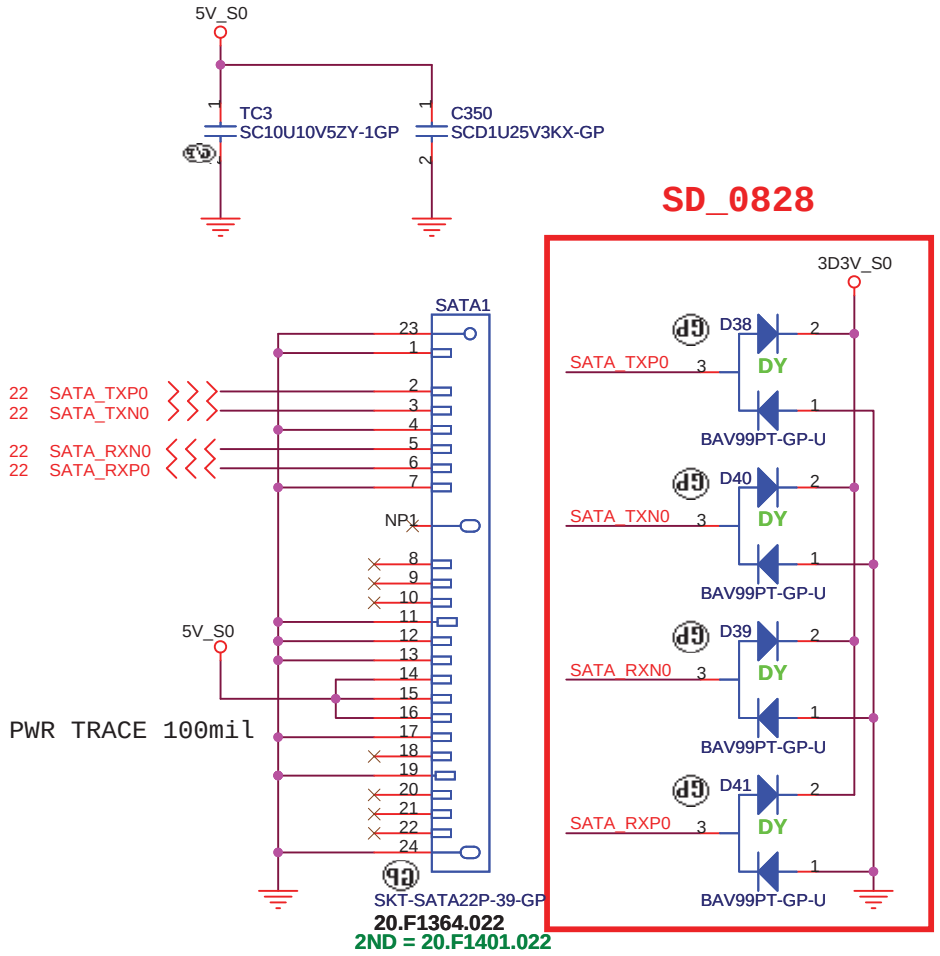
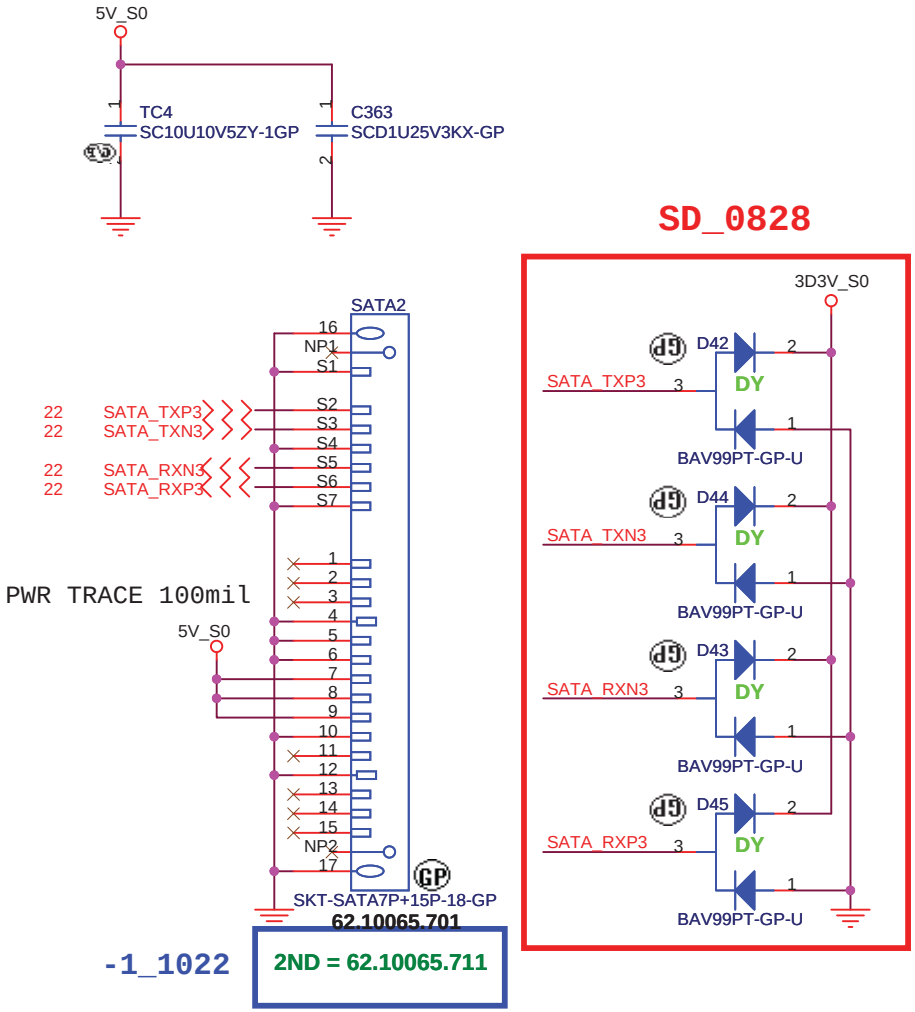
SATA HDD Connector



2ND SATA HDD Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD	
Size A4	Document Number Big Bear 2A	Rev SD
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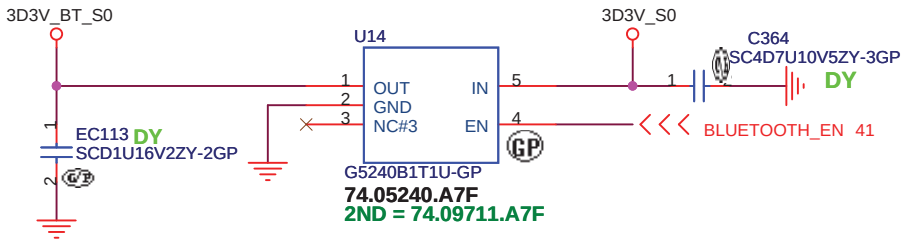
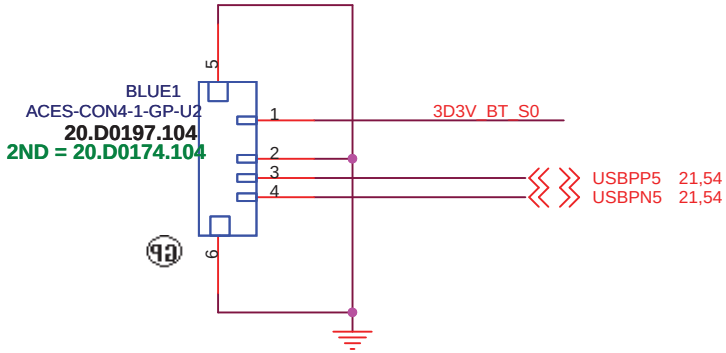
BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request



<Core Design>

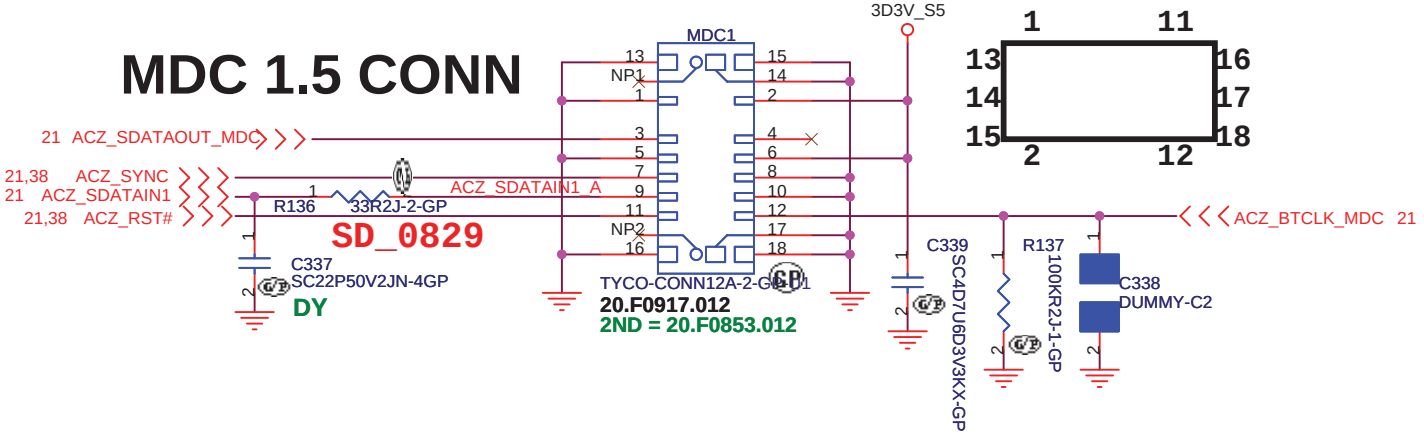
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH

Size	Document Number	Rev
A4	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 28 of 55

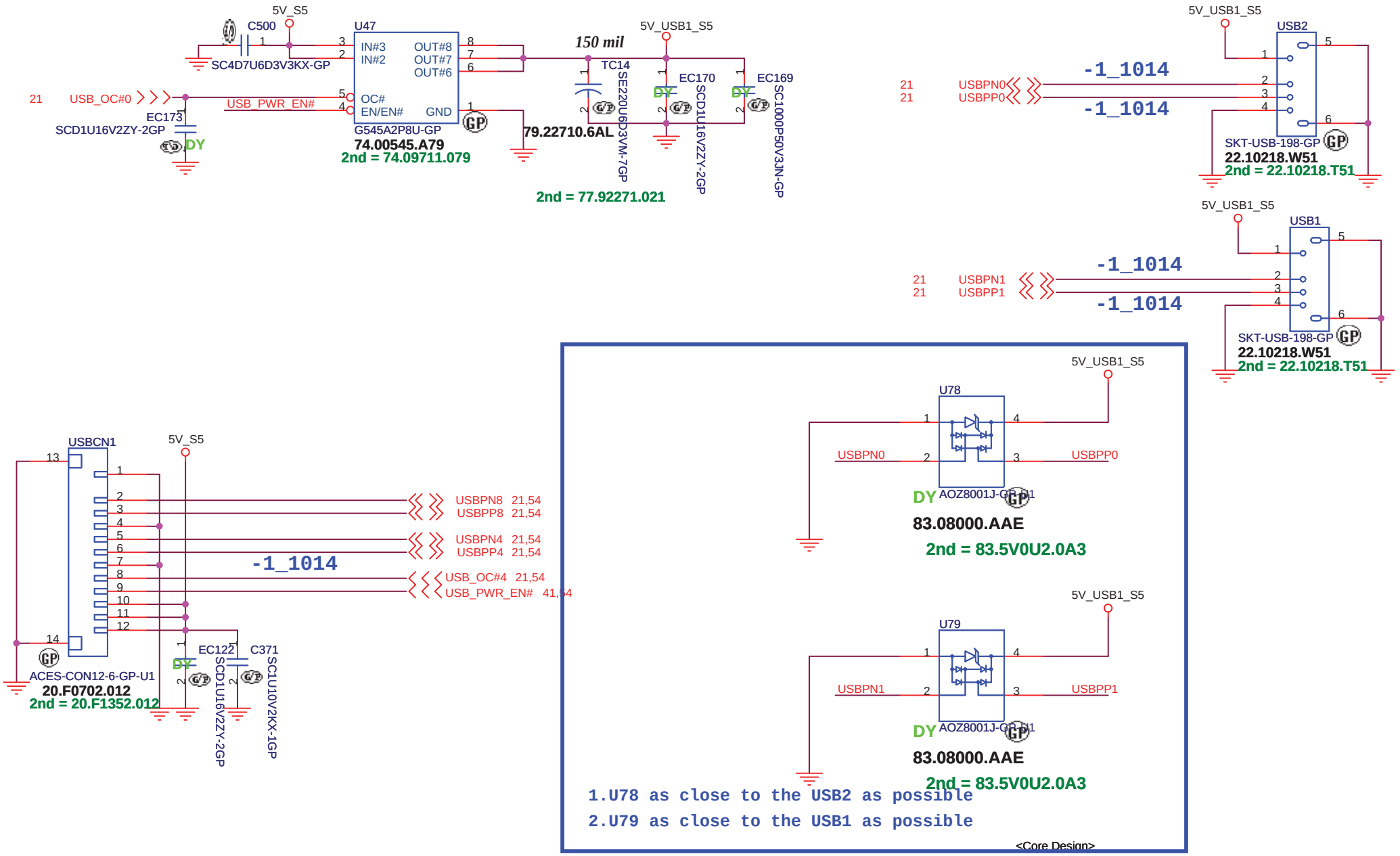
MDC 1.5 CONN



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MDC		
Size: A4	Document Number: Big Bear 2A	Rev: SA
Date: Monday, October 27, 2008	Sheet 29 of 55	

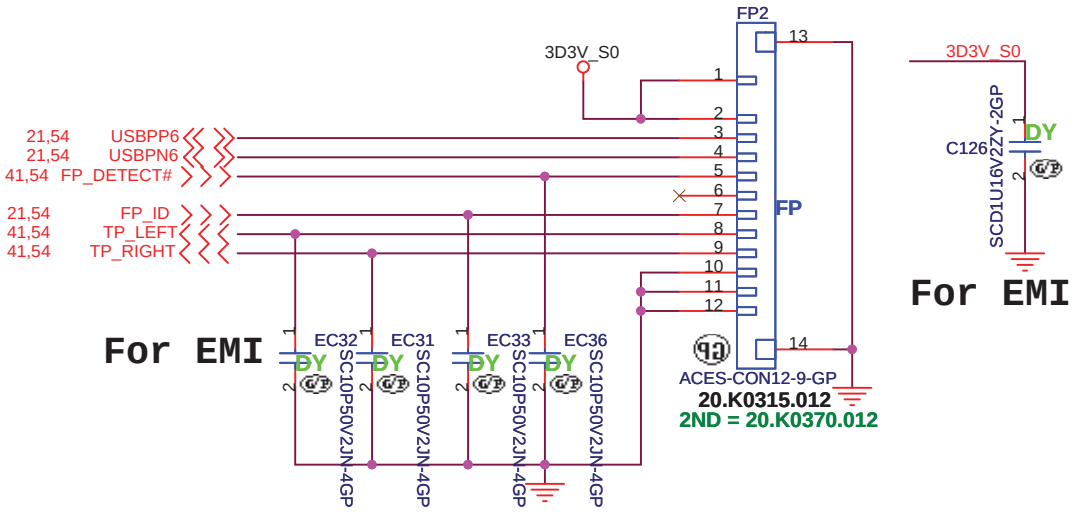


ESD Protection

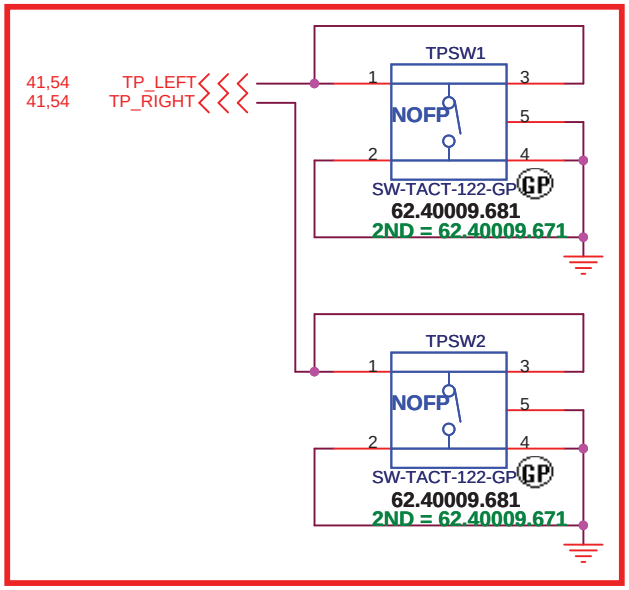
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size A4	Document Number Big Bear 2A	Rev SB
Date: Monday, October 27, 2008	Sheet 30 of 55	

Finger printer



SD_0903



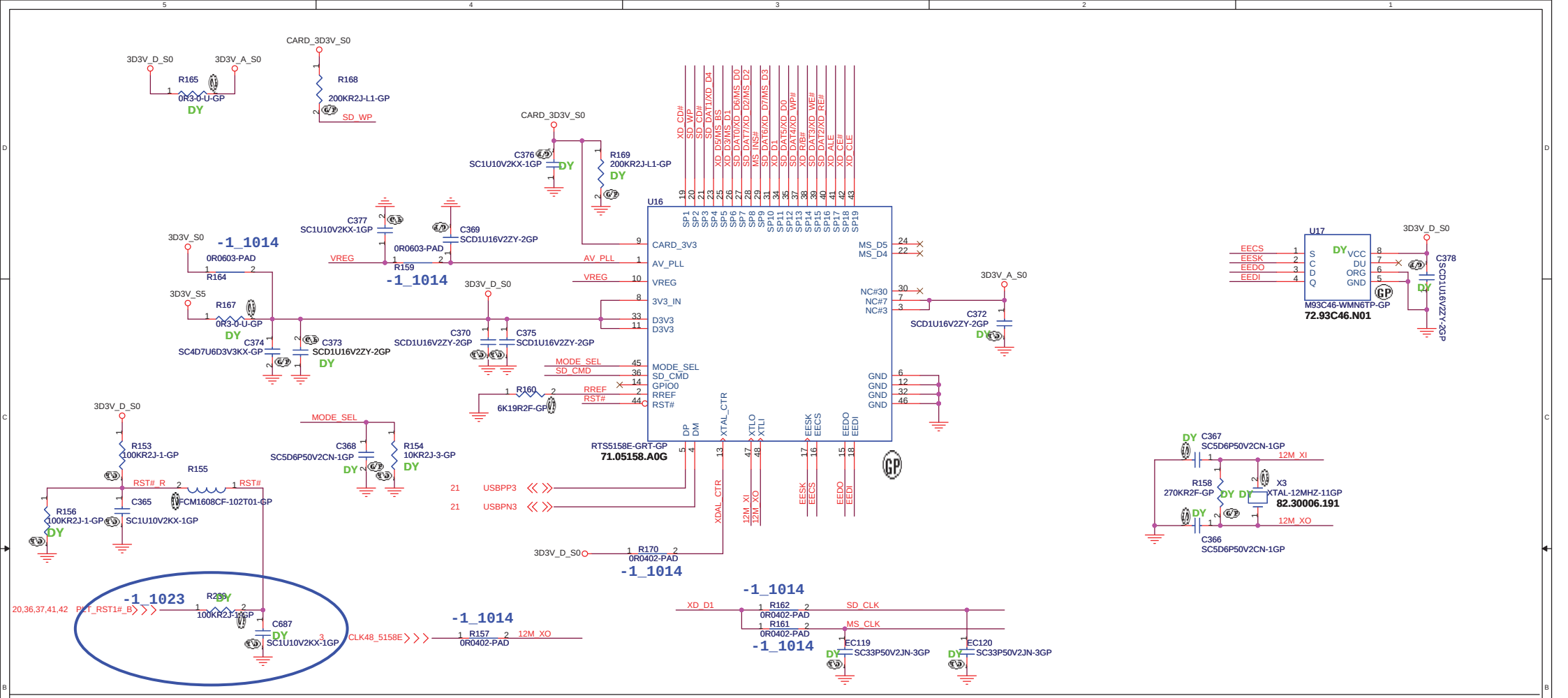
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

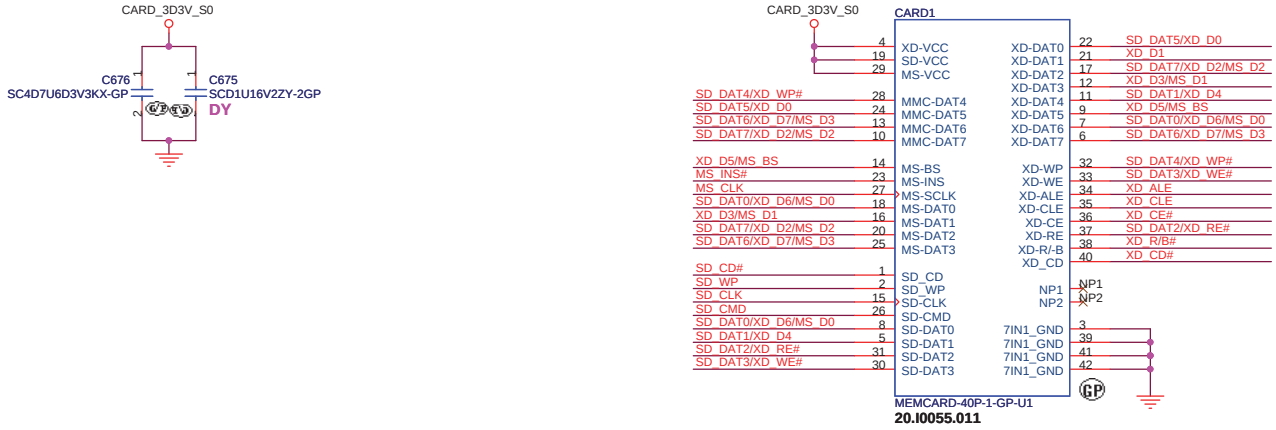
Title: *Finger Printer*

Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 31 of 55



7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

Wistron Corporation
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Title: *Card Reader Connector*

Size	Document Number	Rev
A3	Big Bear 2A	SD

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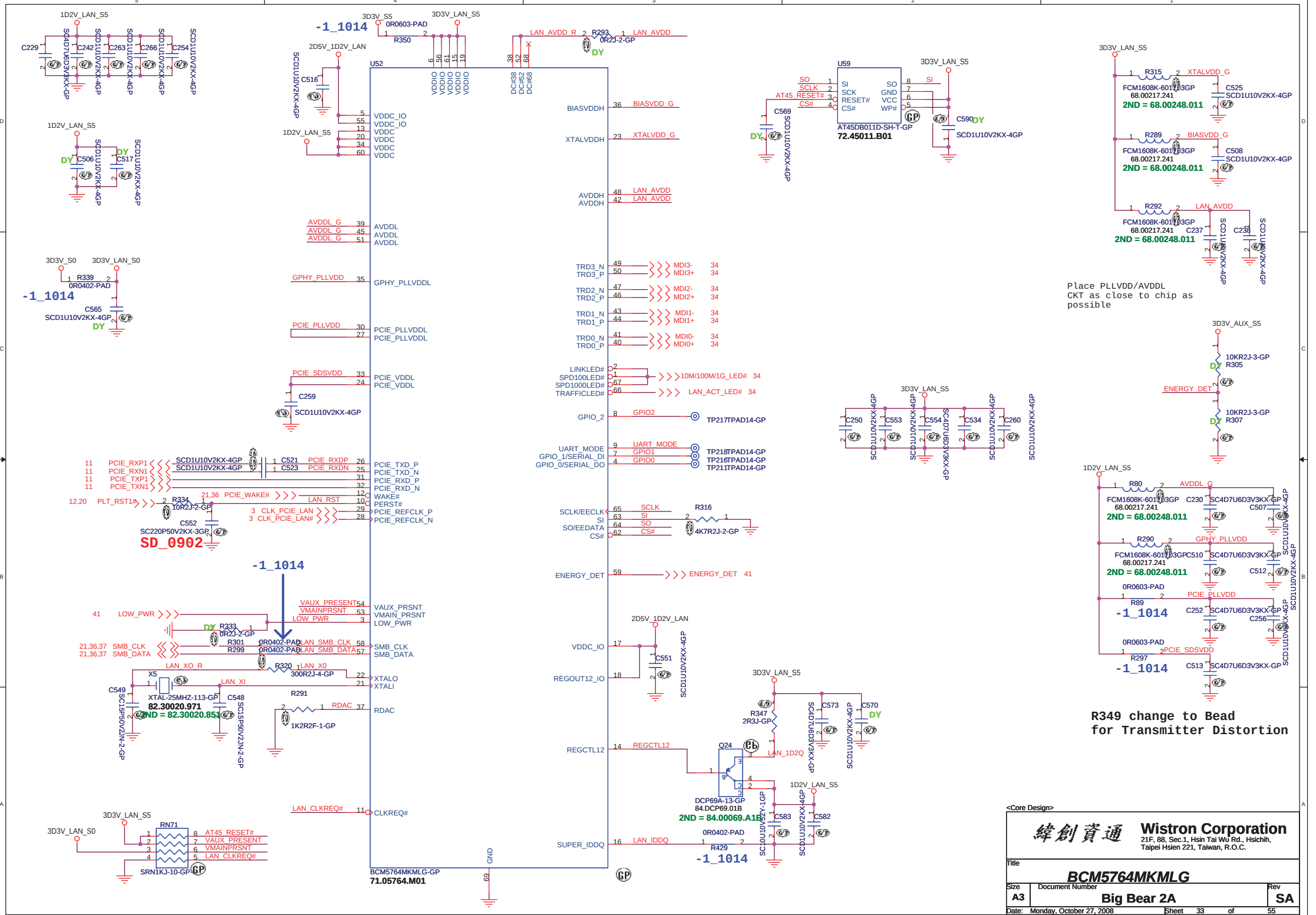
U52
BCM5764MKMLG-GP
71.05764.M01
U59
AT45DB011D-SH-T-GP
72.45011.B01
-1_1014
SD_0902
2ND = 68.00248.011
2ND = 82.30020.851
82.30020.971
2ND = 84.00069.A1B
DCP69A-13-GP
84.DCP69.01B
XTAL-25MHZ-113-GP
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R349 change to Bead
for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size
A3
Document Number
Big Bear 2A
Rev
SA
Date: Monday, October 27, 2008
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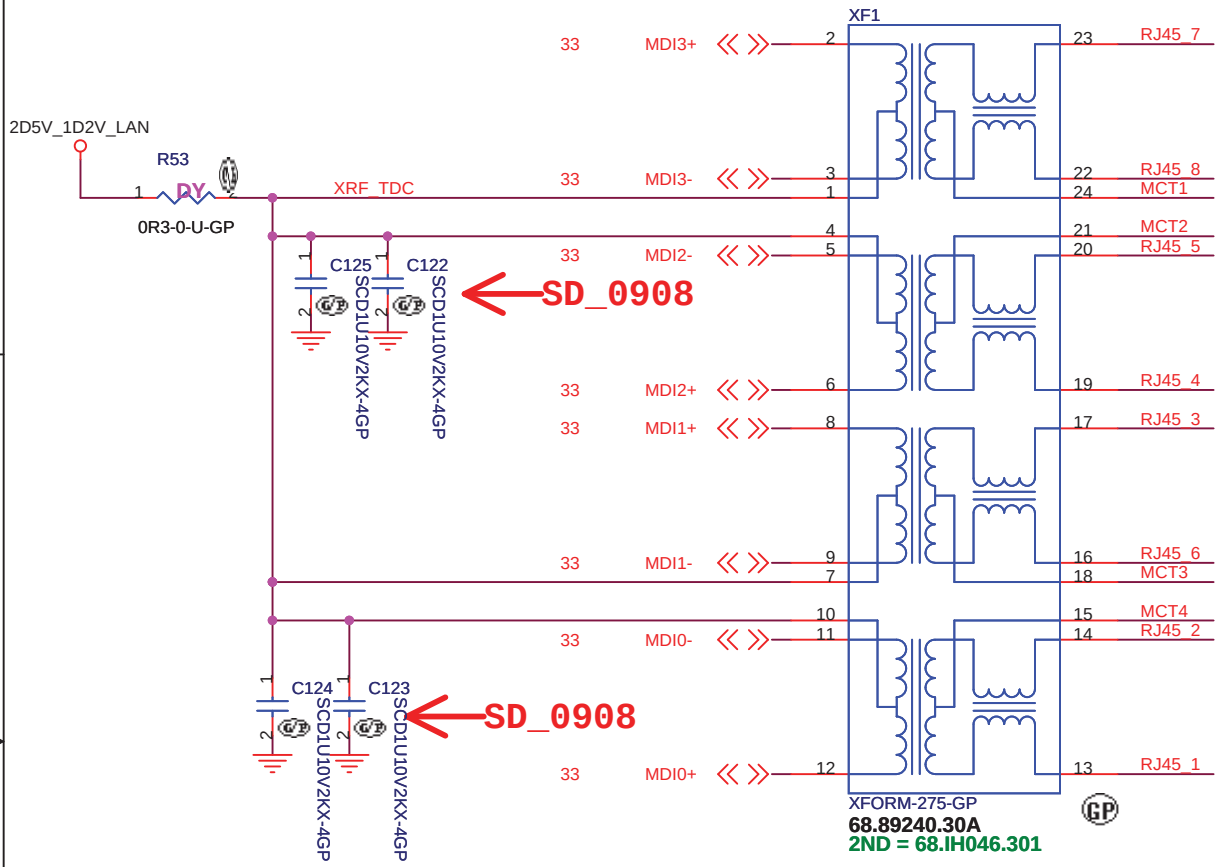
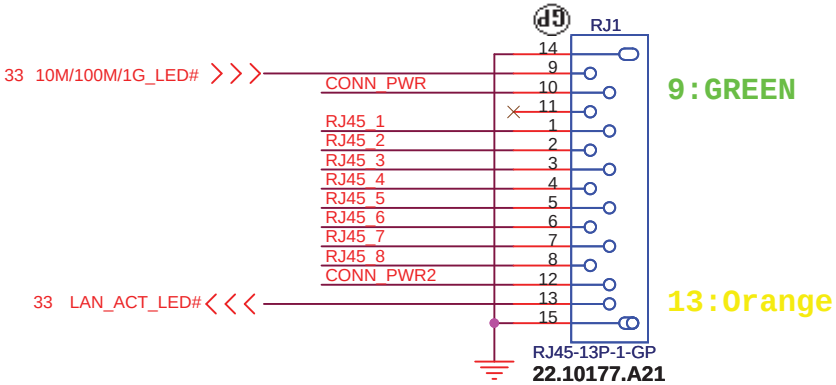
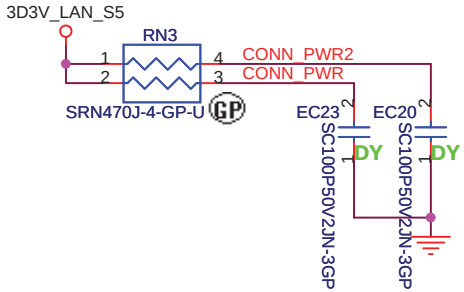
LAN Connector

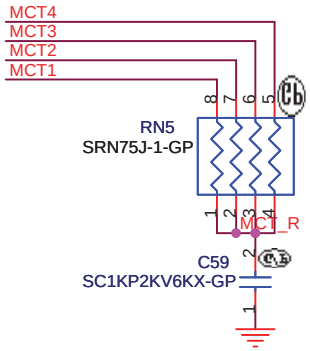




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

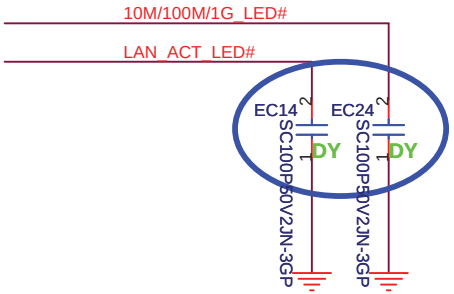
LAN Data: Yellow(B2), when LAN is transfering data.





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size: A4	Document Number: Big Bear 2A	Rev: SB
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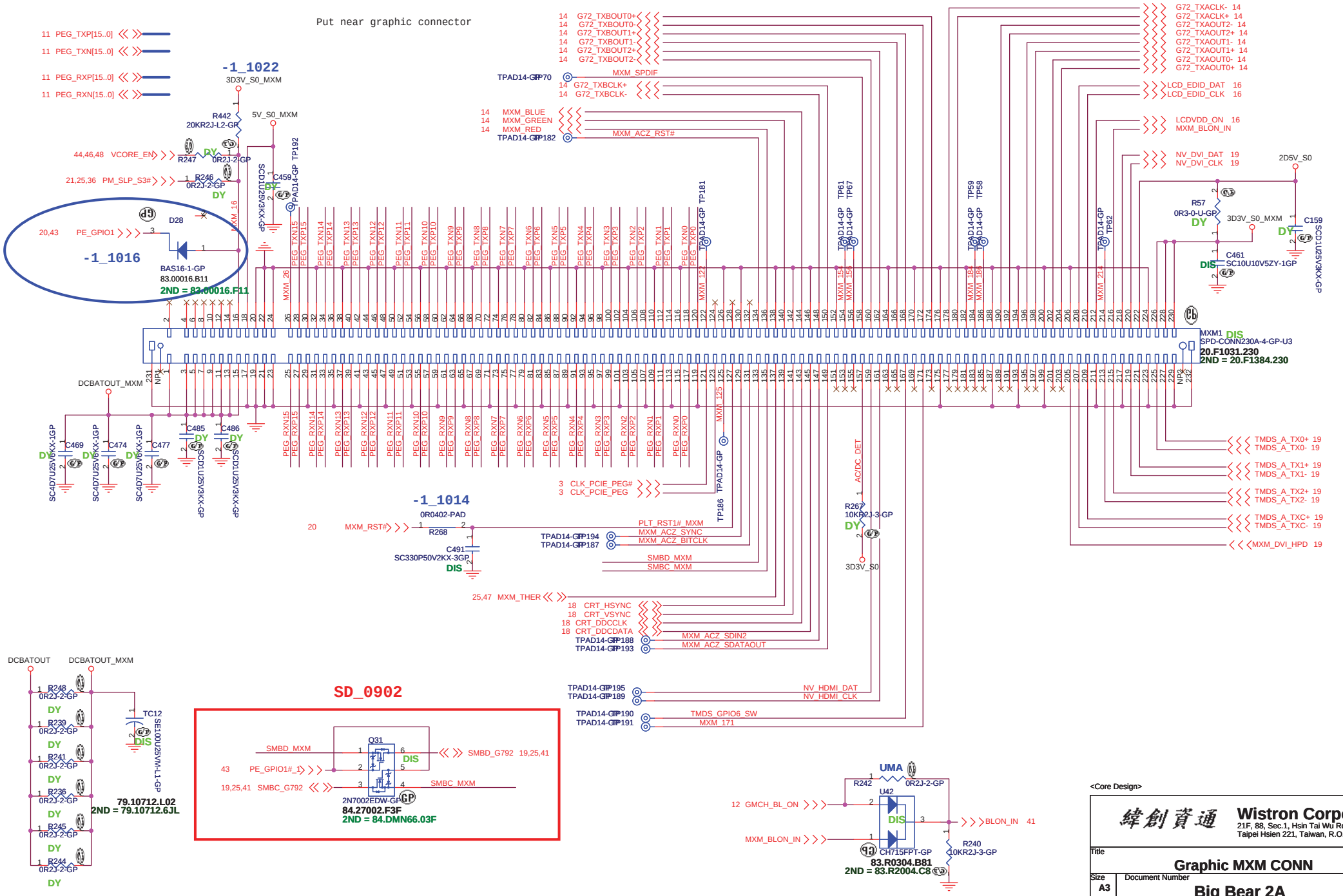
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS
Put near graphic connector
-1_1022
-1_1016
-1_1014
SD_0902
MXM1
SPD-CONN230A-4-GP-U3
20.F1031.230
2ND = 20.F1384.230
BAS16-1-GP
83.00016.B11
2ND = 83.00016.F11
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
CH715FPT-GP
83.R0304.B81
2ND = 83.R2004.C8
79.10712.L02
2ND = 79.10712.6JL
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM CONN
Big Bear 2A
Size A3
Rev SD
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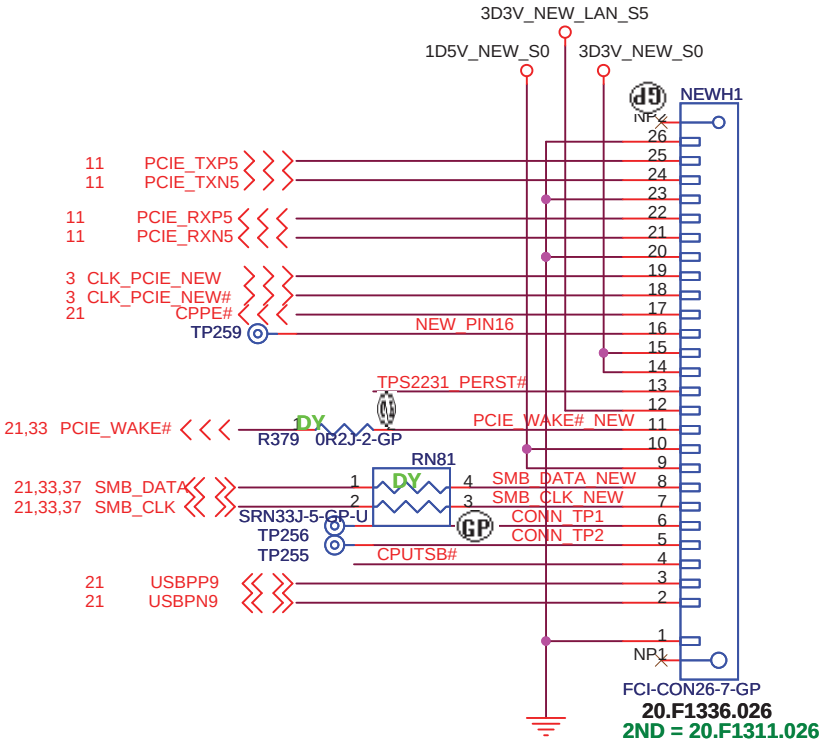
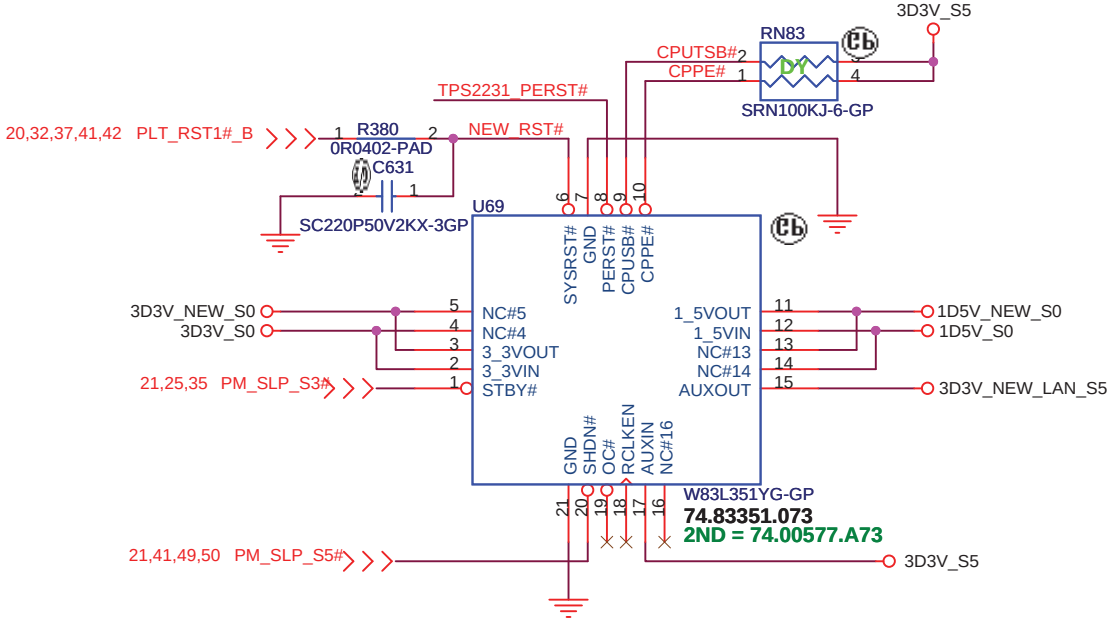
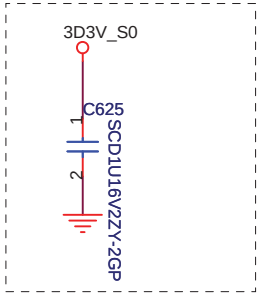
NEWCARD Connector

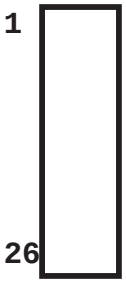


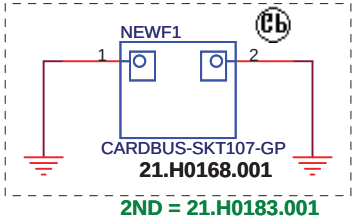


Place them Near to Chip

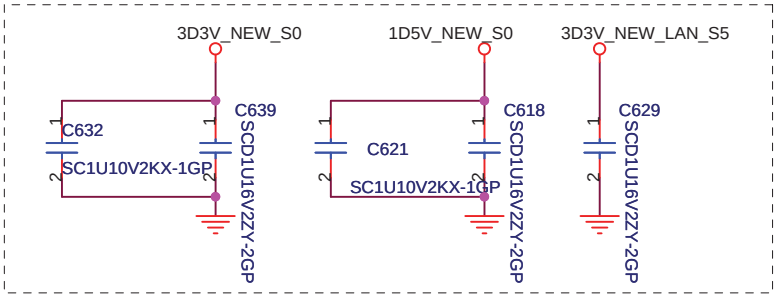


TOP VIEW





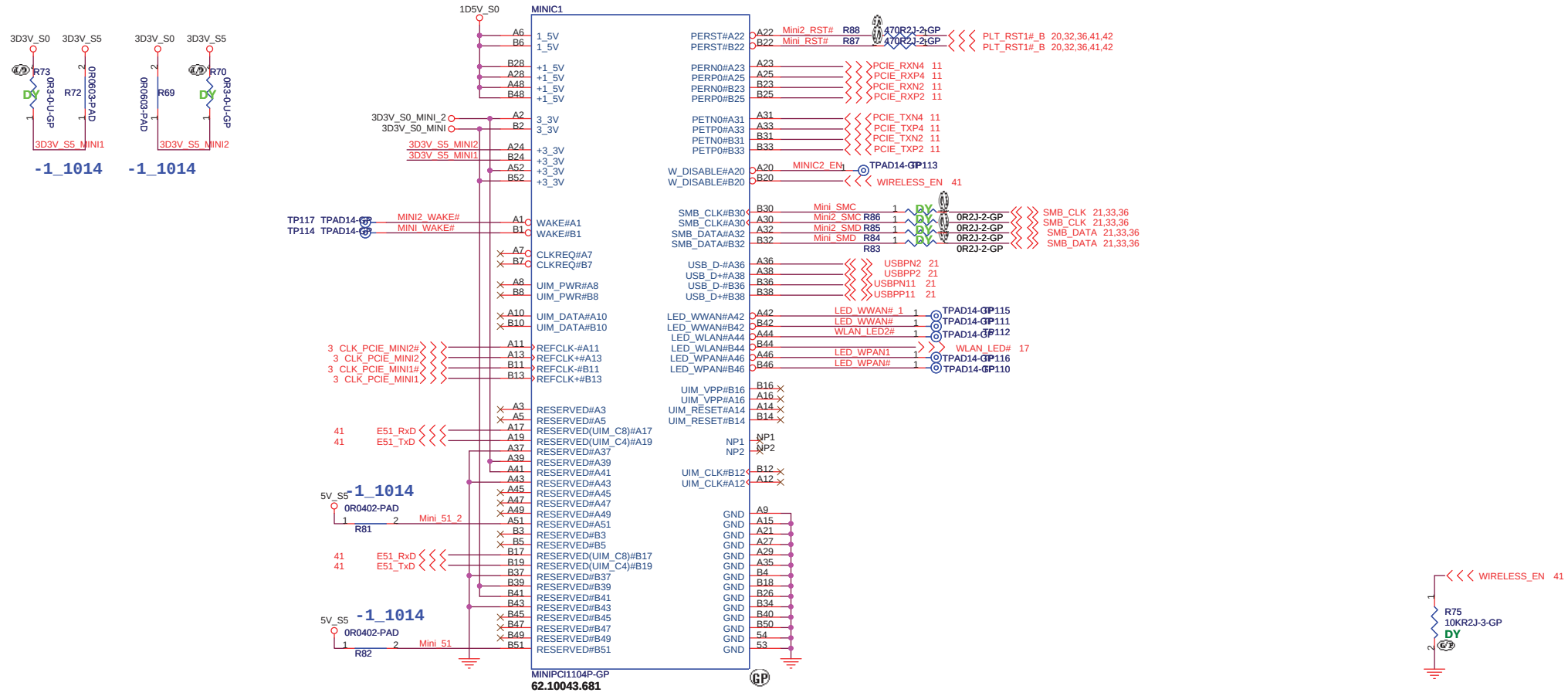
Place them Near to Connector



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	NEW CARD	
Size A4	Document Number Big Bear 2A	Rev SC
Date: Monday, October 27, 2008	Sheet 36 of 55	

Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT



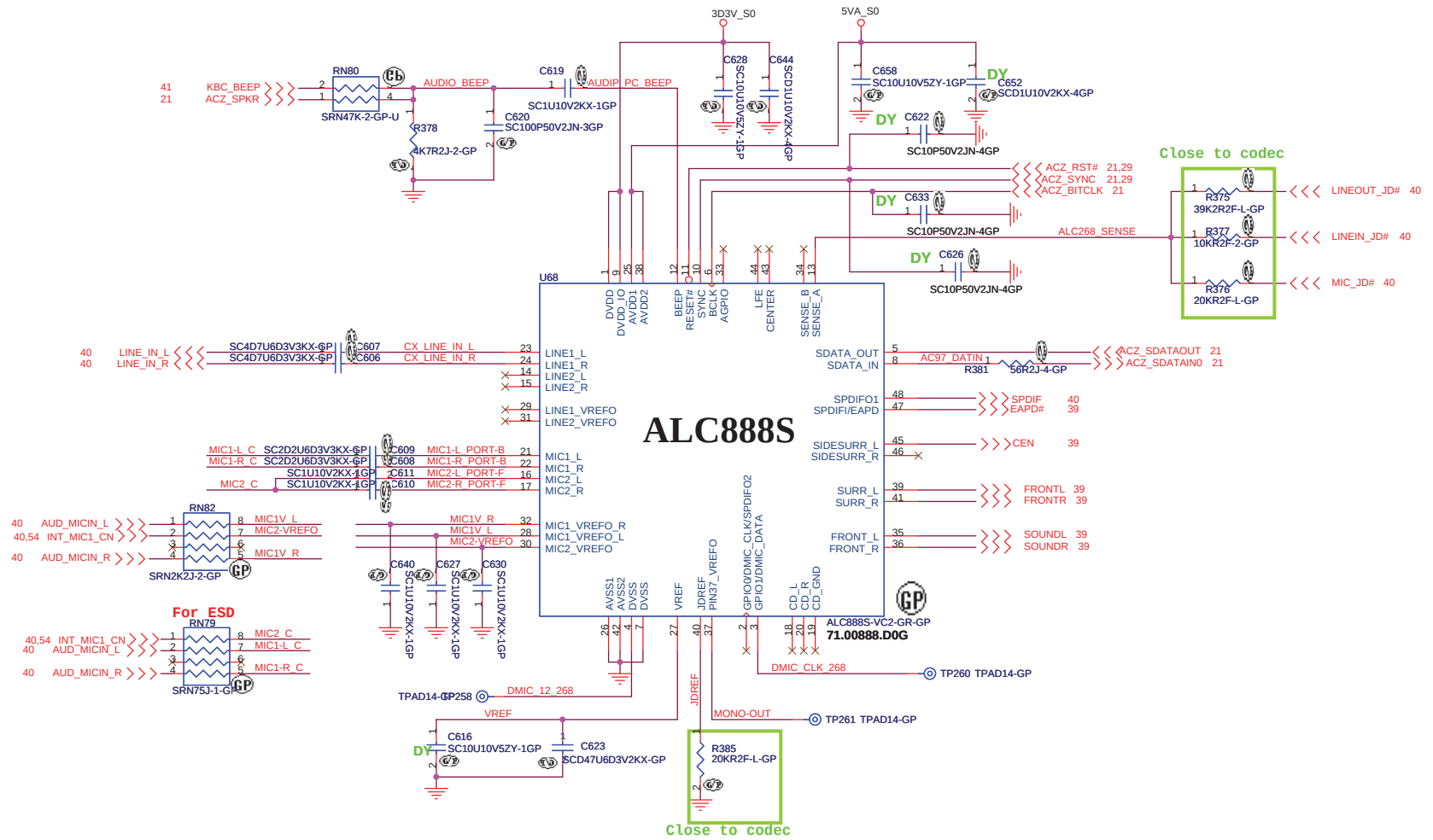
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card**

Size: A3 | Document Number: **Big Bear 2A** | Rev: SA

Date: Monday, October 27, 2008 | Sheet 37 of 55



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC268***

Size	Document Number	Rev
A3	Big Bear 2A	SA

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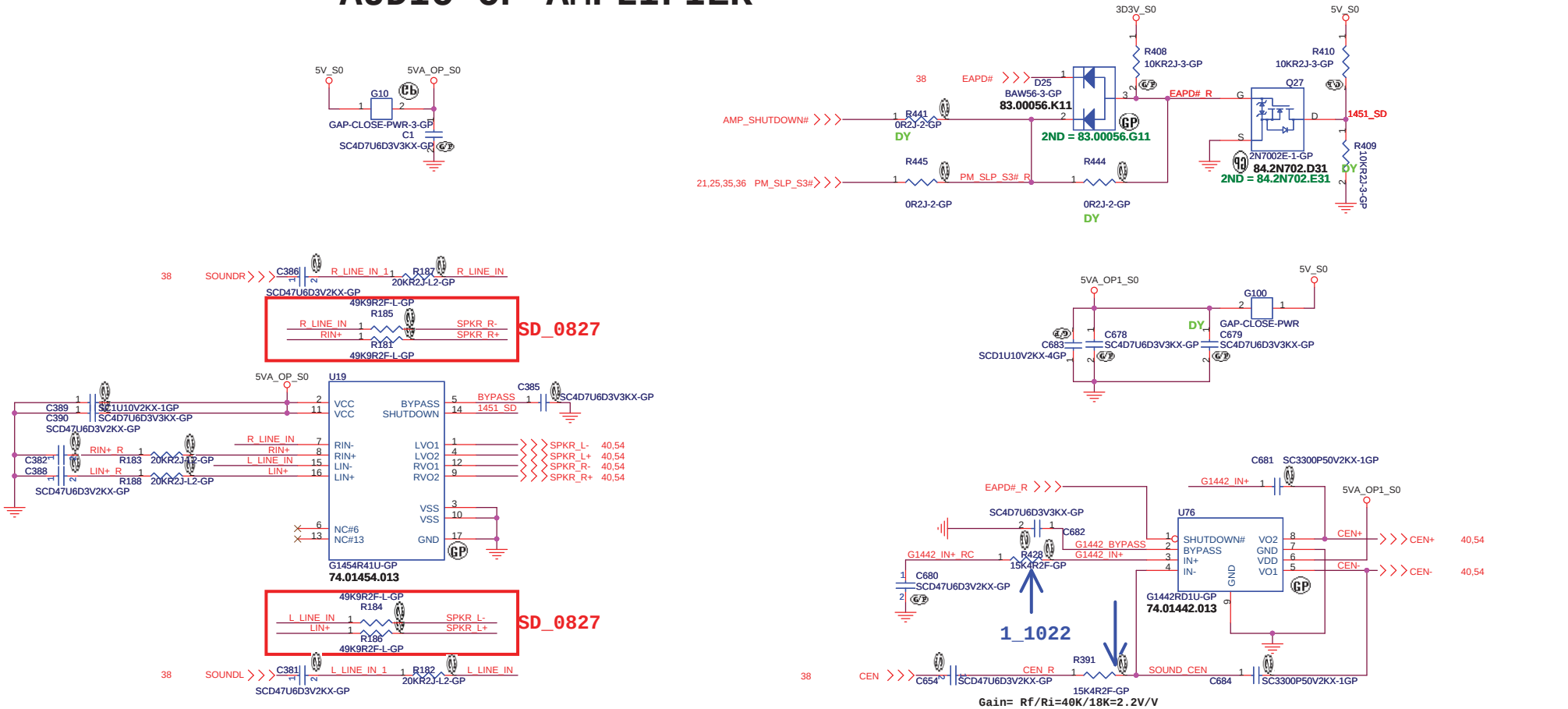
AUDIO OP AMPLIFIER

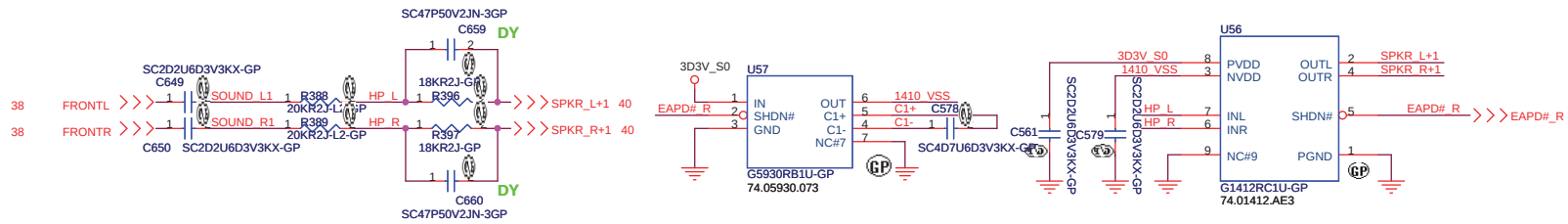


Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W

Gain= Rf/Ri=40K/18K=2.2V/V
f(HP)=1/(2 Pi*18K*0.47uf)=18Hz
If VIN= 1.54V Gain=2.2V/V RL=4Ω VO(peak) =3.38V V(rms)=2.390V
Power= 2.390^2/4=1.428W

Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?

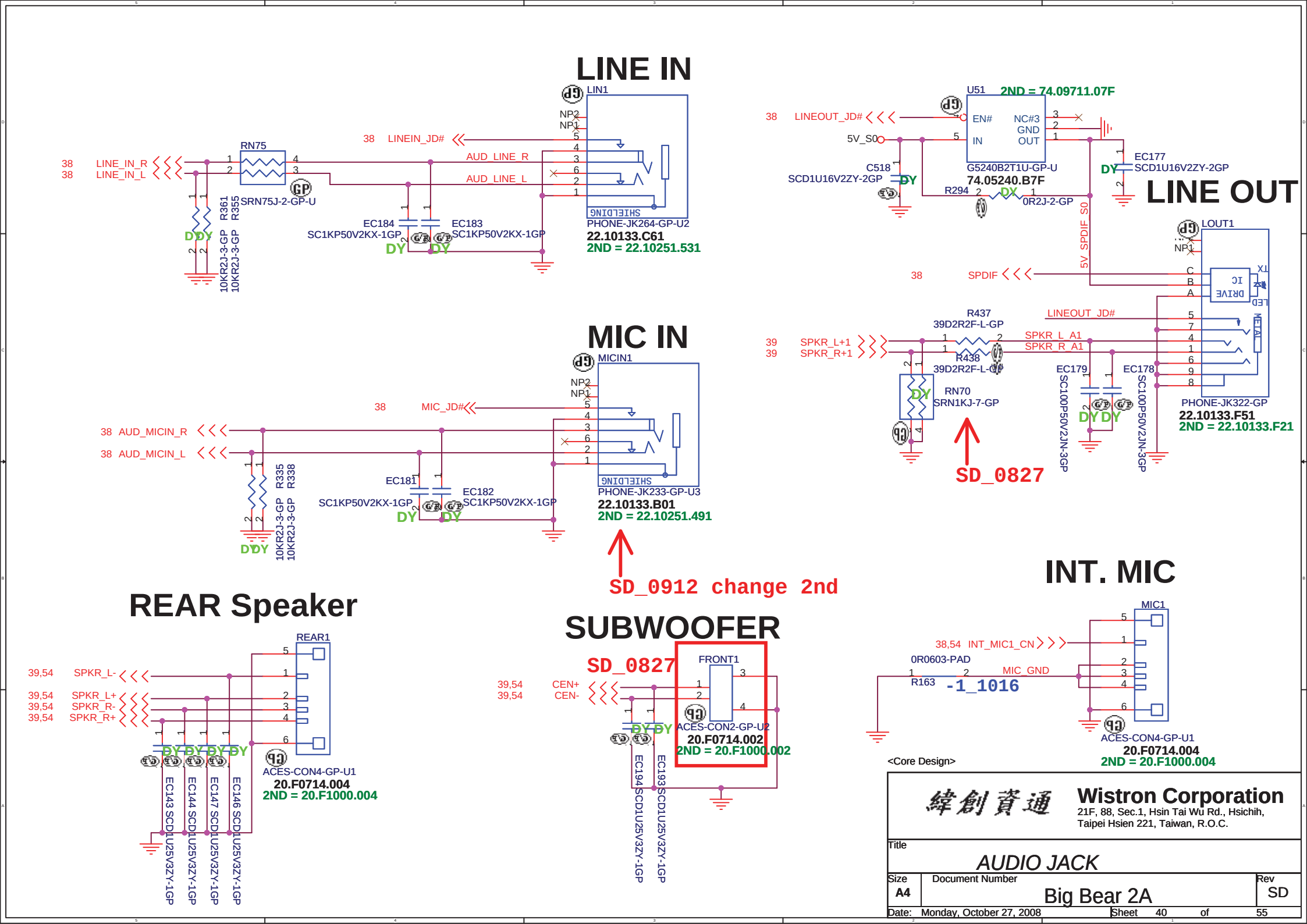
KBC_MUTE_GPIO8



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size A3	Document Number Big Bear 2A	Rev SB
Date: Monday, October 27, 2008	Sheet 39 of 55	



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO JACK*

Size	Document Number	Rev
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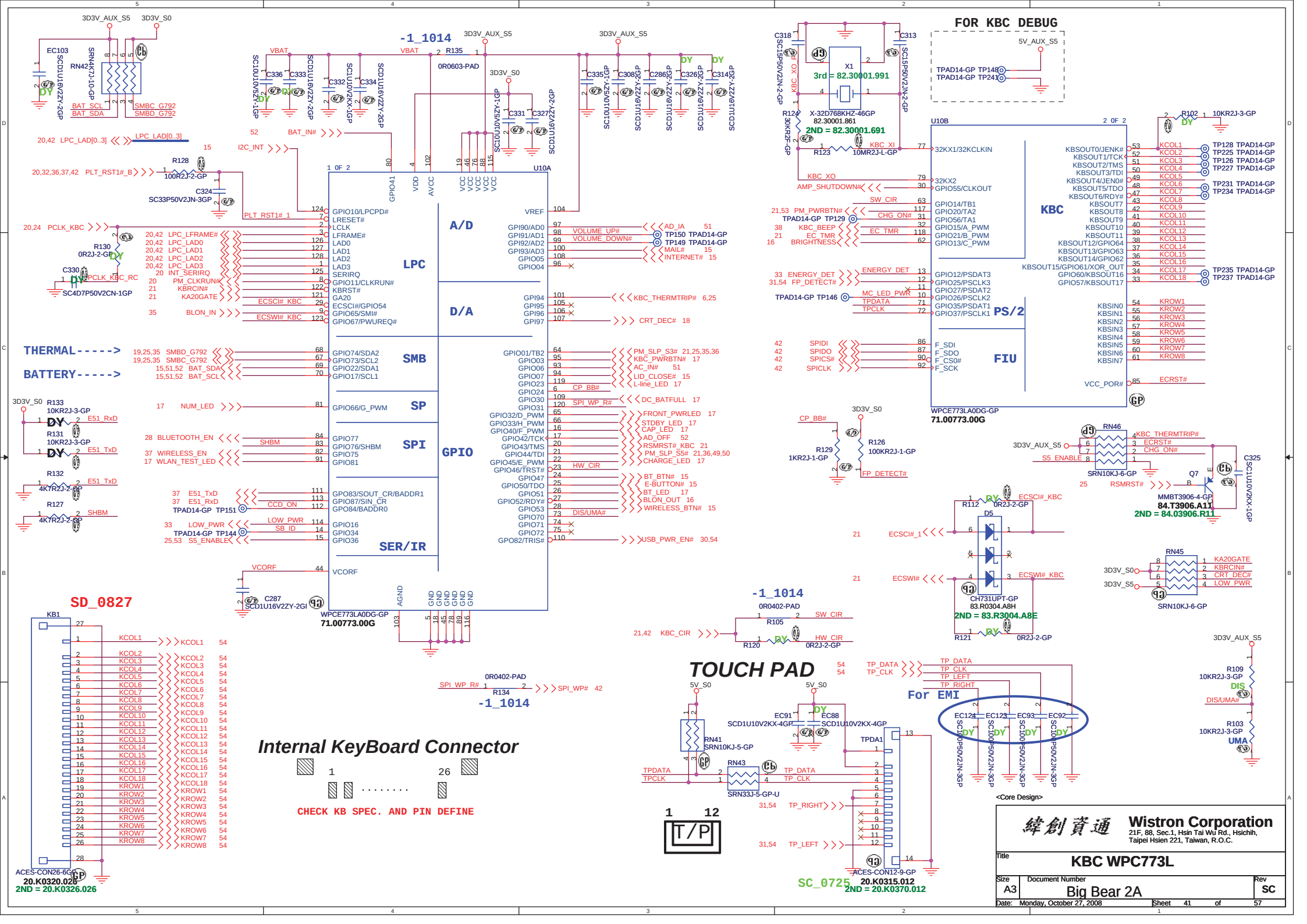
FOR KBC DEBUG
-1_1014
U10A
WPCE773LA0DG-GP
71.00773.00G
U10B
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
SD_0827
KB1
ACES-CON26-6G
20.K0320.026
2ND = 20.K0326.026
Internal KeyBoard Connector
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
For EMI
ACES-CON12-9-G
SC_0725
20.K0315.012
2ND = 20.K0370.012
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC773L
Size
A3
Document Number
Big Bear 2A
Rev
SC
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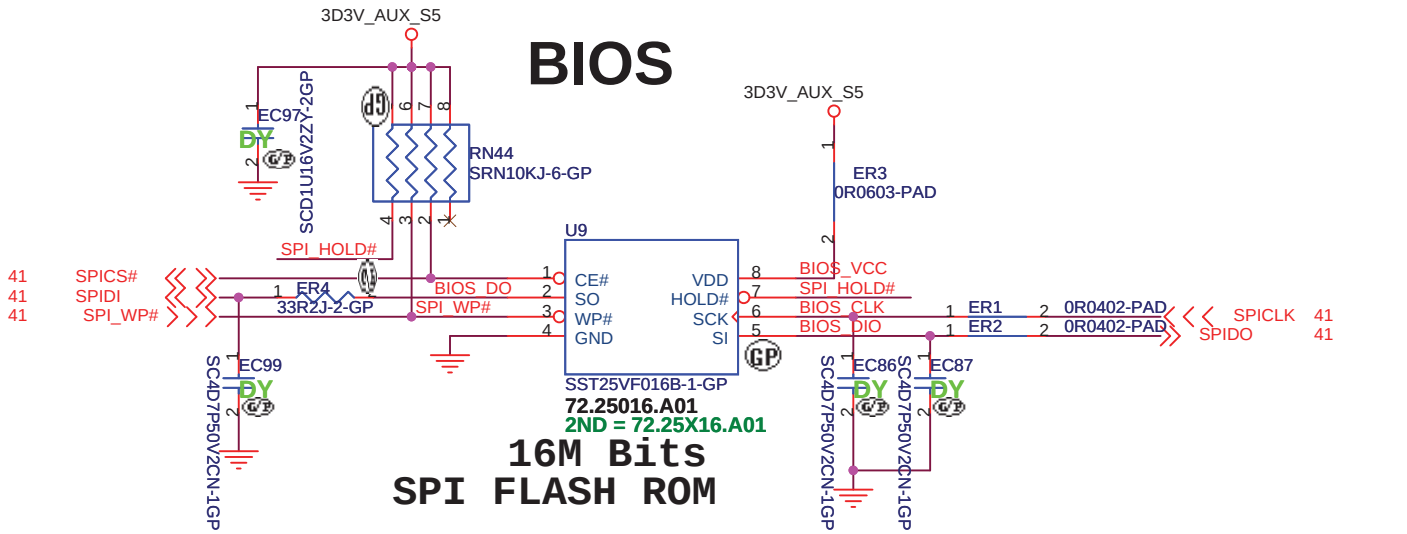
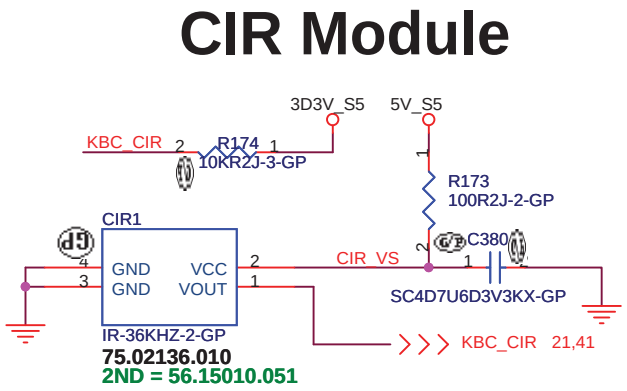
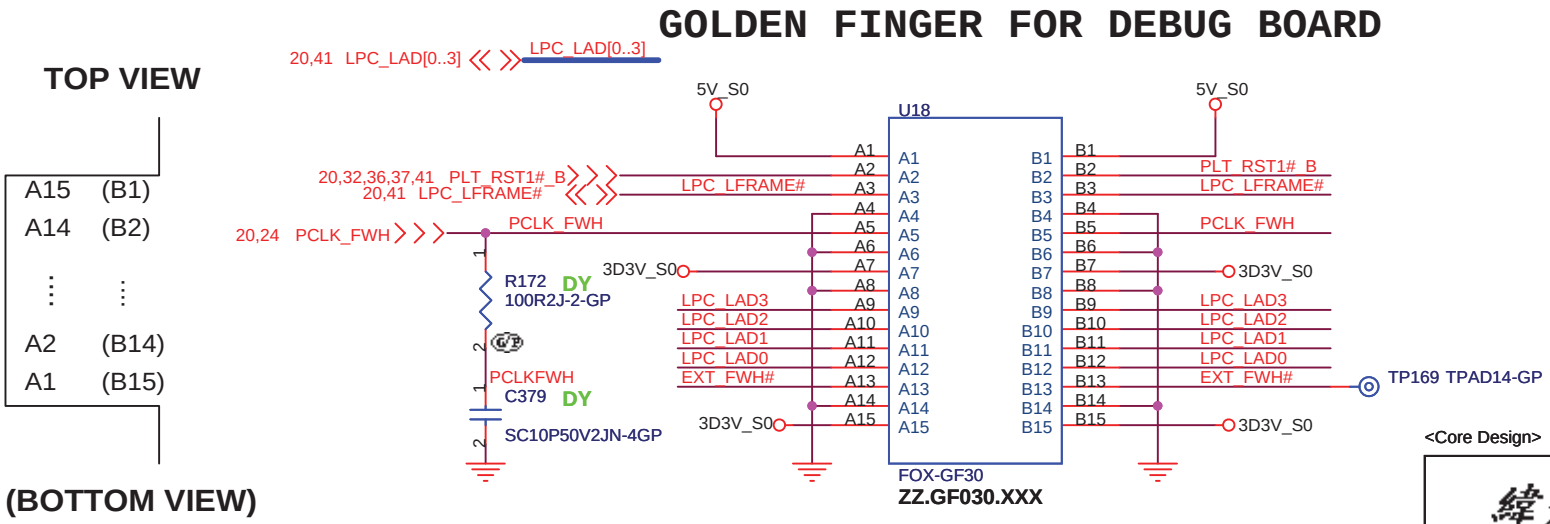


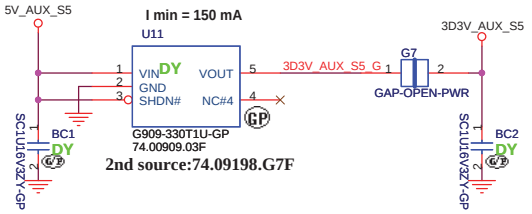




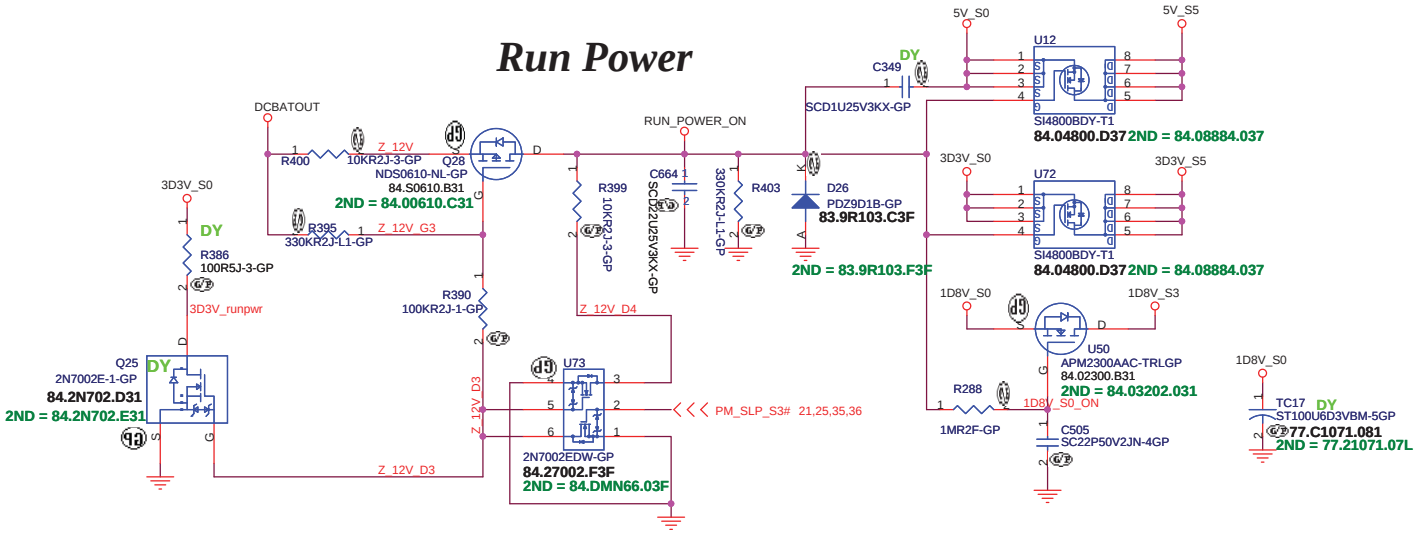
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS & CIR***	
Size A4	Document Number **Big Bear 2A**	Rev SB
Date: Monday, October 27, 2008	Sheet 42 of 57	

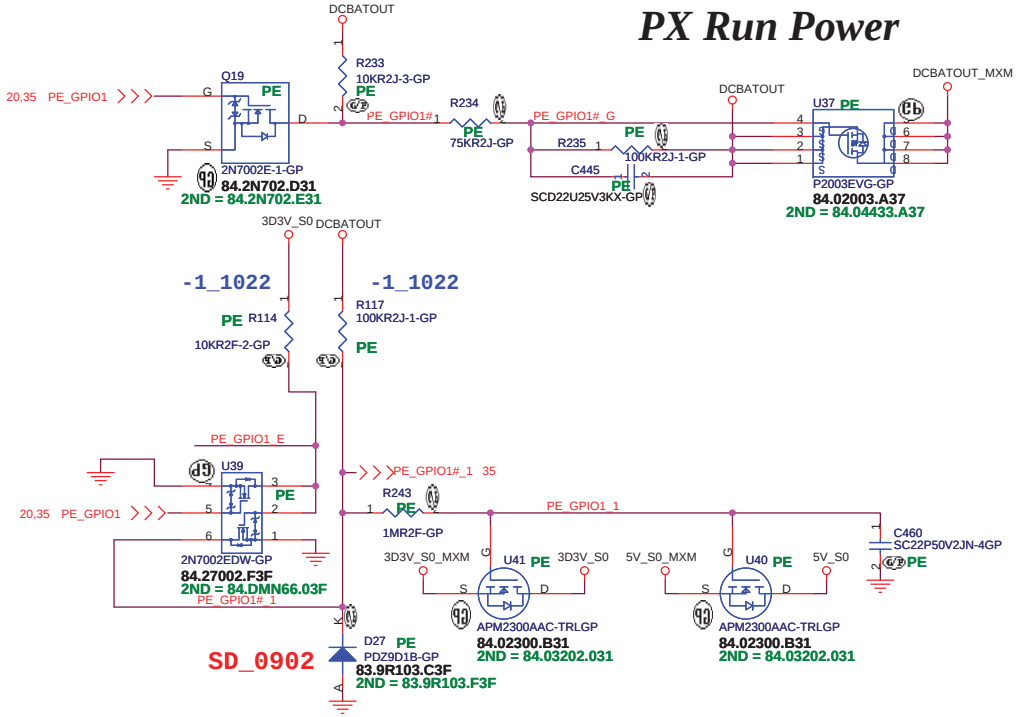
Aux Power 3D3V_AUX_S5



Run Power

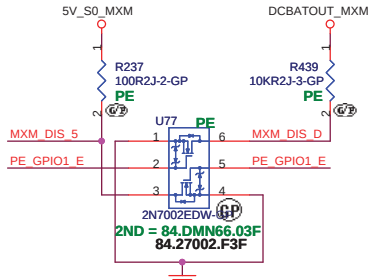


PX Run Power



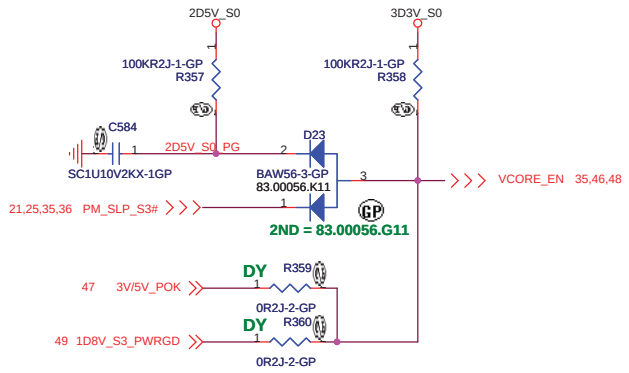
SD_0902

PX Run Power Discharge circuit

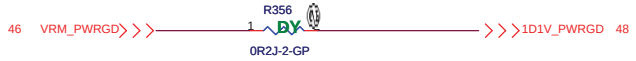


<Core Design>

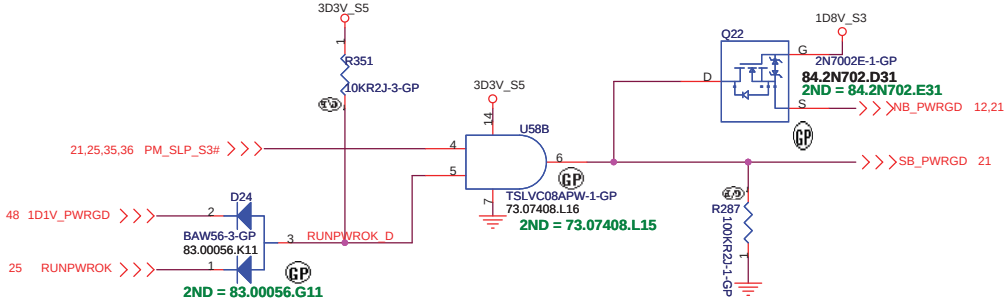
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5	
Size A3	Document Number Big Bear 2A	Rev SD
Date: Monday, October 27, 2008	Sheet 43 of 57	



P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

Size	Document Number	Rev
A3	Big Bear 2A	SA

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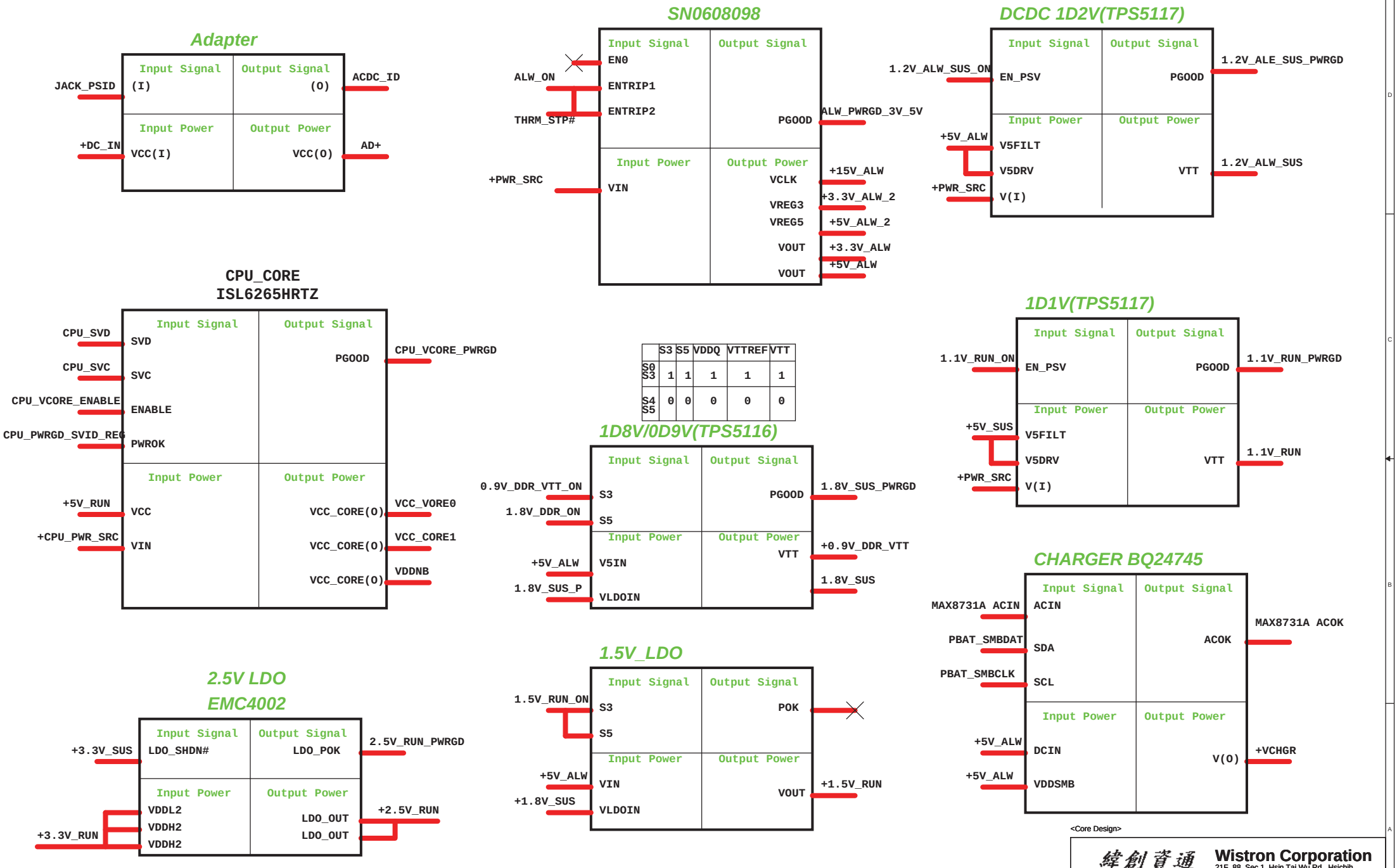
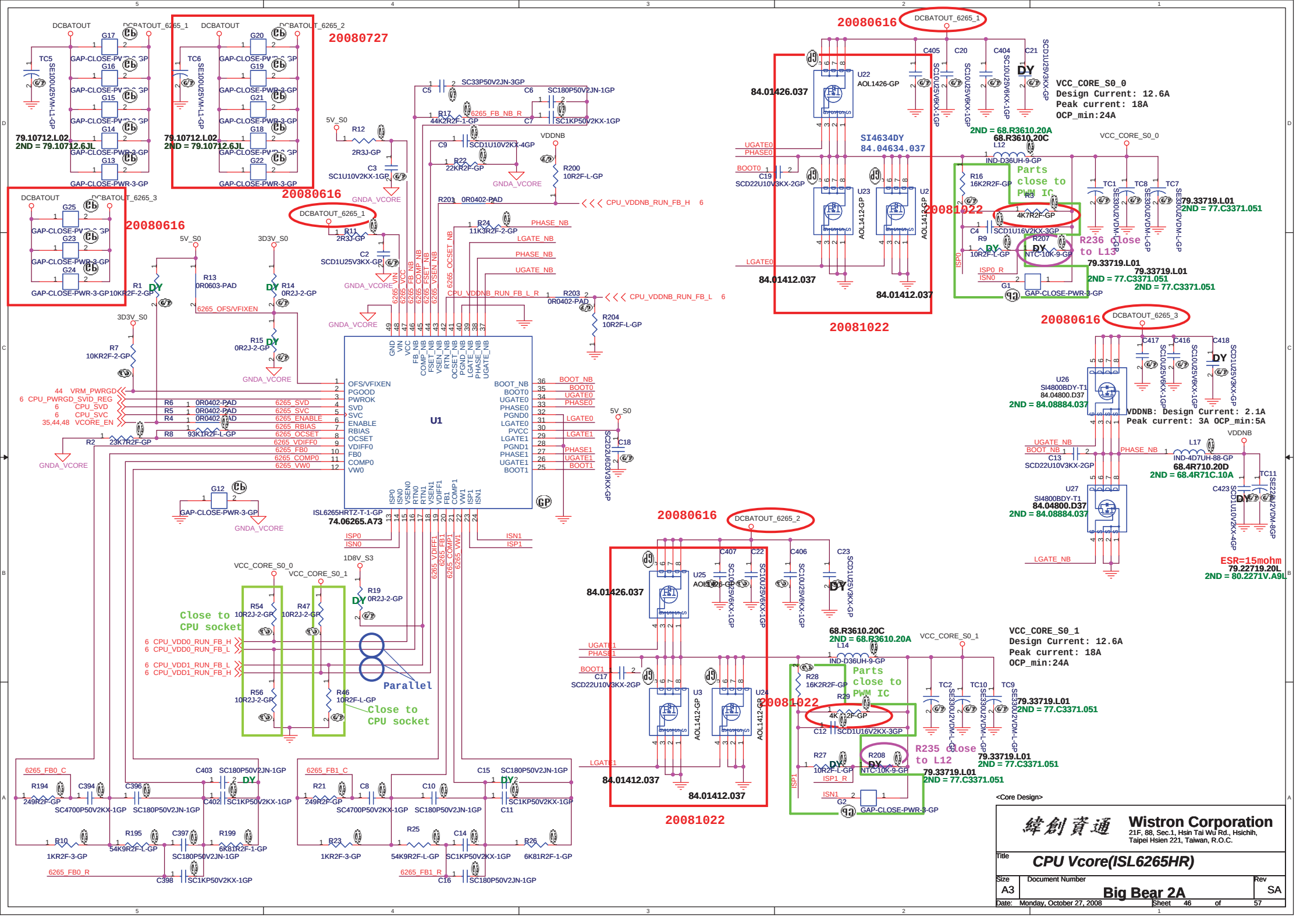
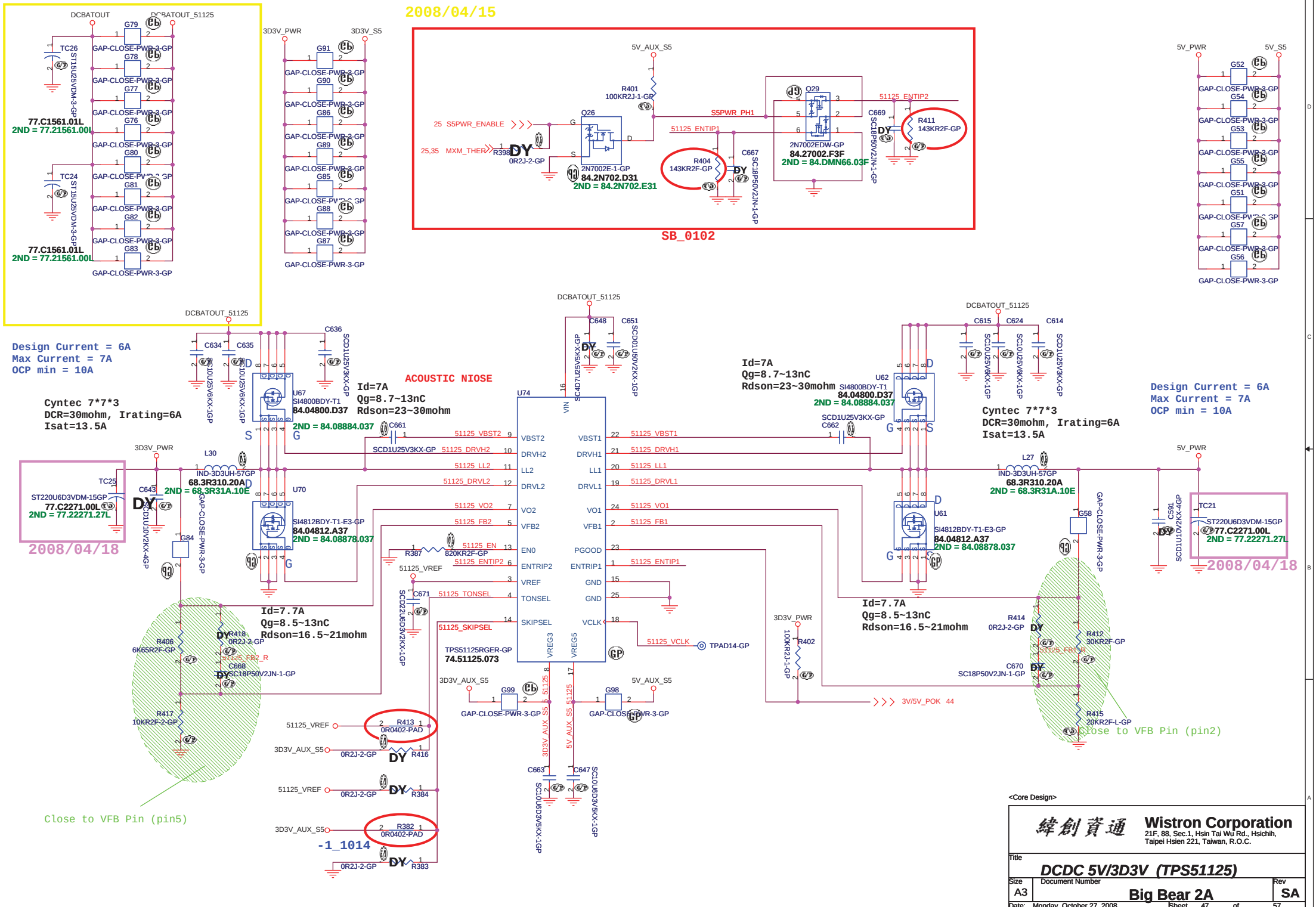
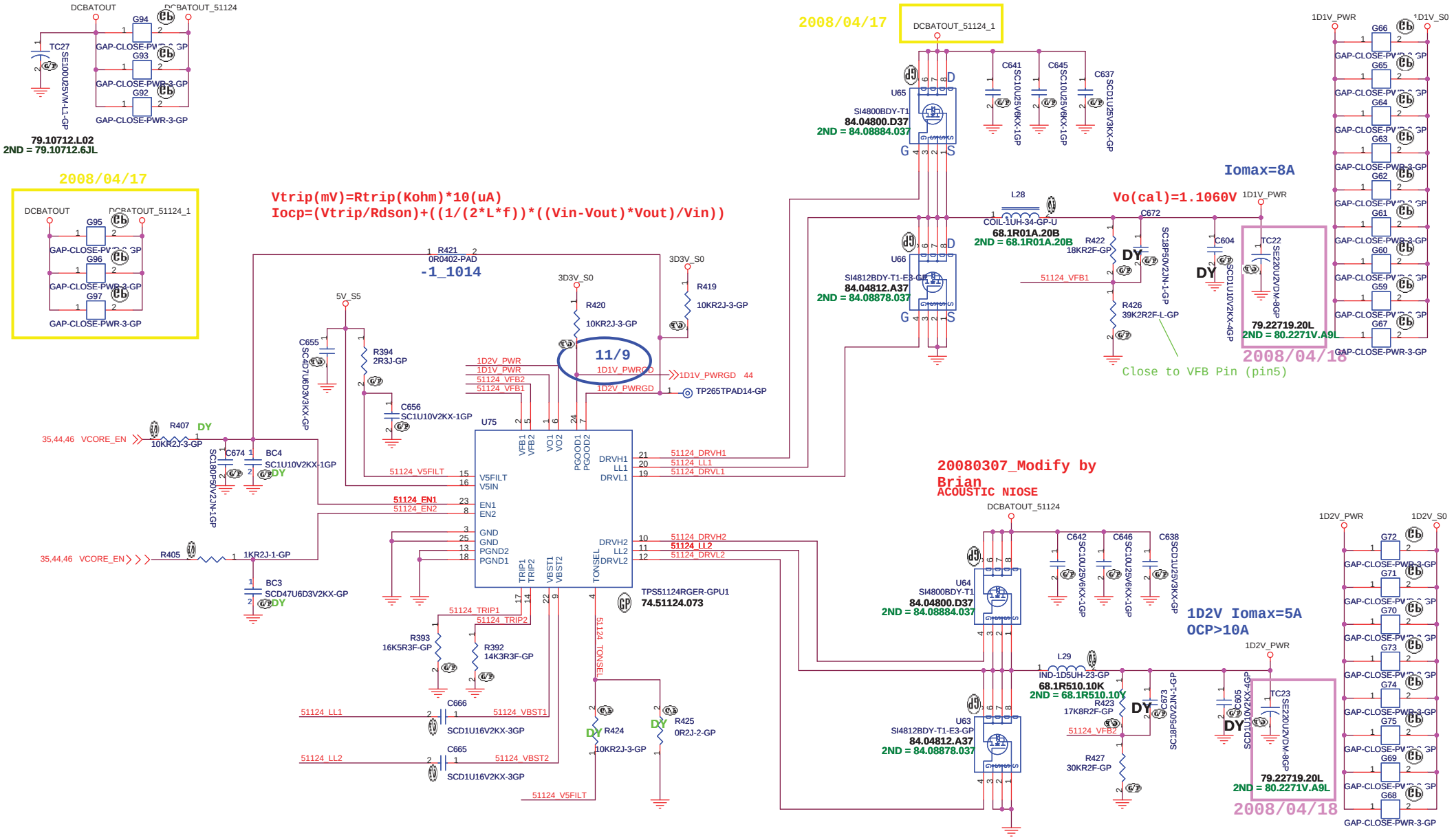

Adapter
Input Signal
Output Signal
JACK_PSID
(I)
(O)
ACDC_ID
Input Power
Output Power
+DC_IN
VCC(I)
VCC(O)
AD+
SN0608098
Input Signal
Output Signal
EN0
ALW_ON
ENTRIP1
ENTRIP2
THRM_STP#
PGOOD
ALW_PWRGD_3V_5V
Input Power
Output Power
+PWR_SRC
VIN
VCLK
+15V_ALW
VREG3
+3.3V_ALW_2
VREG5
+5V_ALW_2
VOUT
+3.3V_ALW
VOUT
+5V_ALW
DCDC 1D2V(TPS5117)
Input Signal
Output Signal
1.2V_ALW_SUS_ON
EN_PSV
PGOOD
1.2V_ALE_SUS_PWRGD
Input Power
Output Power
+5V_ALW
V5FILT
V5DRV
VTT
1.2V_ALW_SUS
+PWR_SRC
V(I)
CPU_CORE
ISL6265HRTZ
Input Signal
Output Signal
CPU_SVD
SVD
CPU_SVC
SVC
PGOOD
CPU_VCORE_PWRGD
CPU_VCORE_ENABLE
ENABLE
CPU_PWRGD_SVID_REG
PWROK
Input Power
Output Power
+5V_RUN
VCC
VCC_CORE(O)
VCC_VORE0
+CPU_PWR_SRC
VIN
VCC_CORE(O)
VCC_CORE1
VCC_CORE(O)
VDDNB
S3 S5 VDDQ VTTREF VTT
S0 S3 1 1 1 1 1
S4 S5 0 0 0 0 0
1D8V/0D9V(TPS5116)
Input Signal
Output Signal
0.9V_DDR_VTT_ON
S3
PGOOD
1.8V_SUS_PWRGD
1.8V_DDR_ON
S5
Input Power
Output Power
+5V_ALW
V5IN
VTT
+0.9V_DDR_VTT
1.8V_SUS_P
VLDOIN
1.8V_SUS
1D1V(TPS5117)
Input Signal
Output Signal
1.1V_RUN_ON
EN_PSV
PGOOD
1.1V_RUN_PWRGD
Input Power
Output Power
+5V_SUS
V5FILT
V5DRV
VTT
1.1V_RUN
+PWR_SRC
V(I)
CHARGER BQ24745
Input Signal
Output Signal
MAX8731A ACIN
ACIN
MAX8731A ACOK
PBAT_SMBDAT
SDA
ACOK
PBAT_SMBCLK
SCL
Input Power
Output Power
+5V_ALW
DCIN
V(O)
+VCHGR
+5V_ALW
VDDSMB
2.5V LDO
EMC4002
Input Signal
Output Signal
+3.3V_SUS
LDO_SHDN#
LDO_POK
2.5V_RUN_PWRGD
Input Power
Output Power
VDDL2
VDDH2
VDDH2
LDO_OUT
LDO_OUT
+2.5V_RUN
+3.3V_RUN
1.5V_LDO
Input Signal
Output Signal
1.5V_RUN_ON
S3
POK
S5
Input Power
Output Power
+5V_ALW
VIN
VOUT
+1.5V_RUN
+1.8V_SUS
VLDOIN
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size
A3
Document Number
Big Bear 2A
Rev
SA
Date: Monday, October 27, 2008
Sheet 45 of 57


20080727
20080616
20081022
U1
ISL6265HRTZ-T-1-GP
74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Parts close to PWM IC
R236 close to L13
R235 close to L12
Close to CPU socket
Parallel
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Size A3
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 46 of 57


2008/04/15
SB_0102
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
77.C1561.01L
2ND = 77.21561.00L
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
ACOUSTIC NIOSE
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
84.04800.D37
2ND = 84.08884.037
84.27002.F3F
2ND = 84.DMN66.03F
84.2N702.D31
2ND = 84.2N702.E31
68.3R310.20A
2ND = 68.3R31A.10E
84.04812.A37
2ND = 84.08878.037
77.C2271.00L
2ND = 77.22271.27L
2008/04/18
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
-1_1014
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2A
Size A3
Rev SA
Date: Monday, October 27, 2008
Sheet 47 of 57



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

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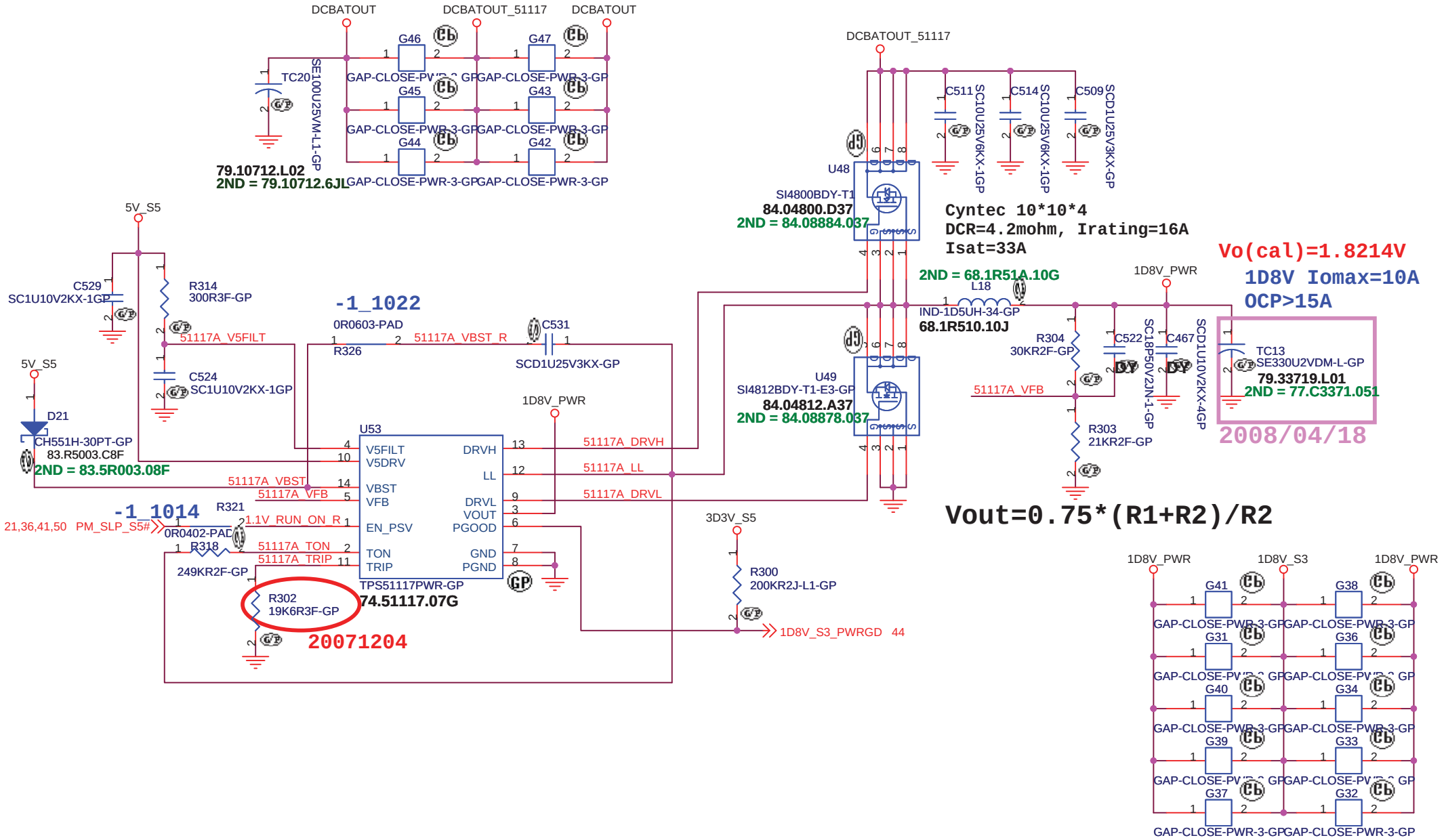
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 48 of 57



<Core Design>

緯創資通 **Wistron Corporation**
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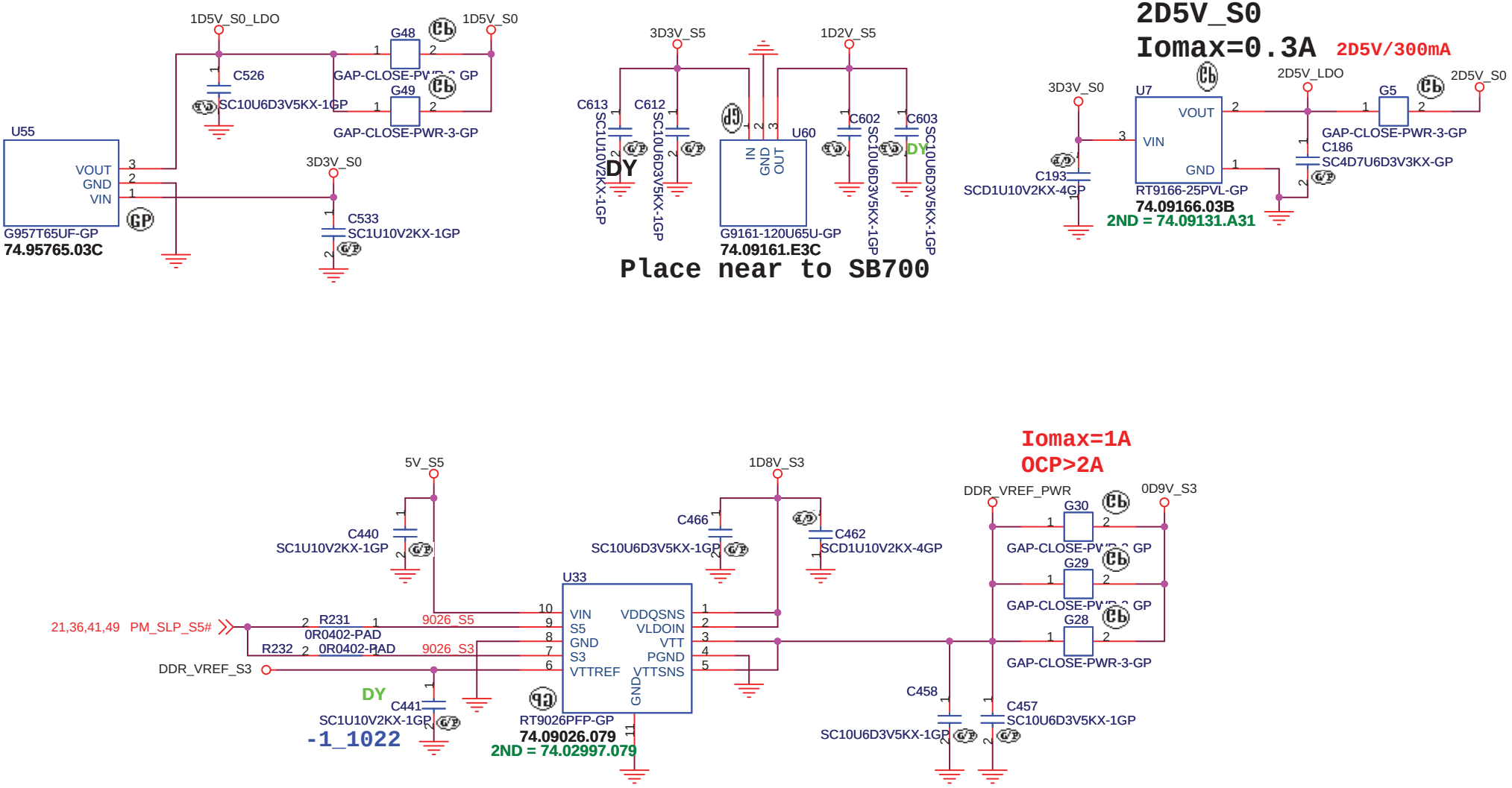
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D8V(TPS5117)	
Size A4	Document Number Big Bear 2A	Rev SB
Date: Monday, October 27, 2008	Sheet 49 of 57	



<Core Design>

緯創資通 **Wistron Corporation**
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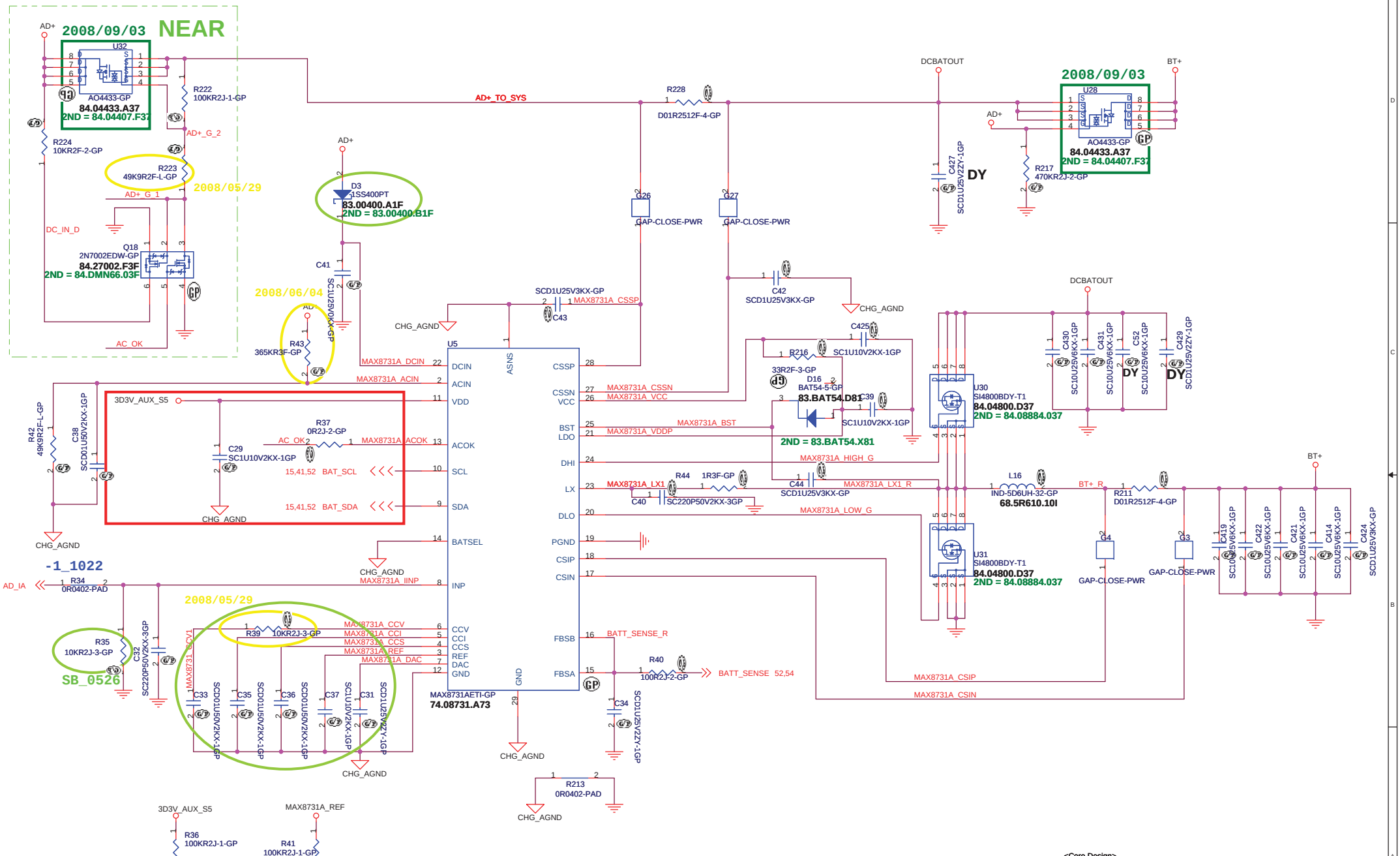
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***0D9V&2D5V&1D25V&1D5V***

Size	Document Number	Rev
A4	**Big Bear 2A**	SB

Date: Monday, October 27, 2008 Sheet 50 of 57



<Core Design>

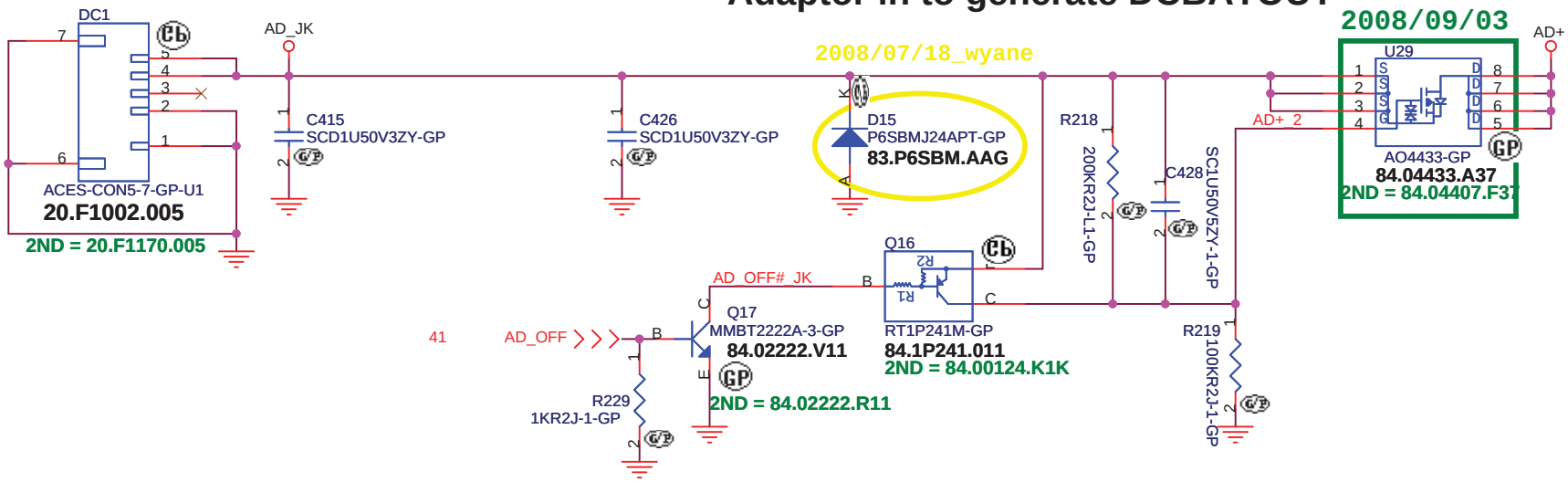
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8731A Charger**

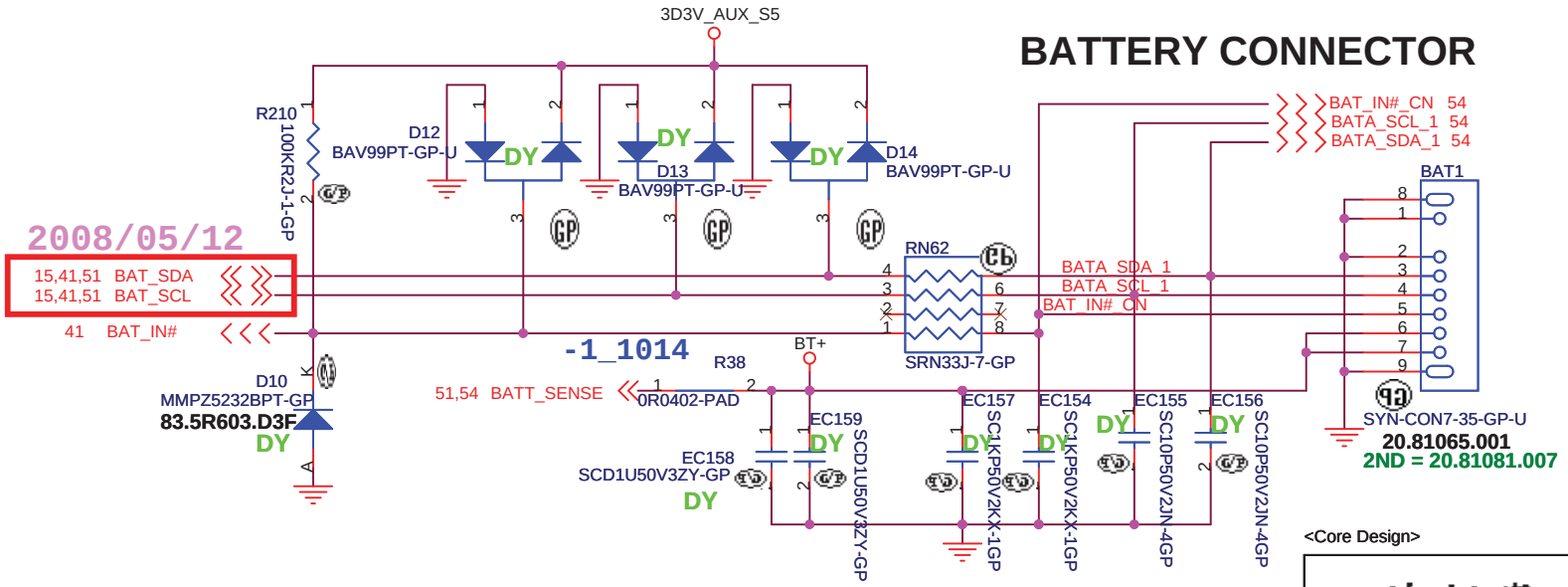
Size: A3 | Document Number: **Big Bear 2A** | Rev: SA

Date: Monday, October 27, 2008 | Sheet 51 of 57

Adaptor in to generate DCBATOUT

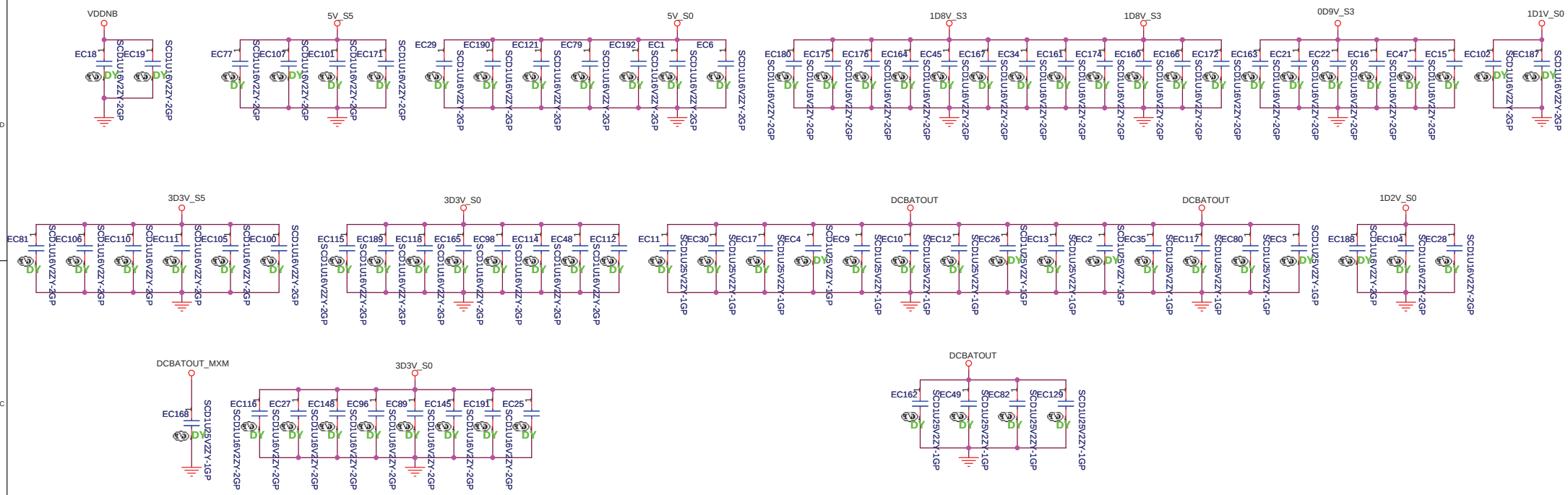


BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size **A4**	Document Number **Big Bear 2A**	Rev SA
Date: Monday, October 27, 2008	Sheet 52 of 57	



SPRING ON BOTTOM

DIMM

GND3 SPRING-62-GP 34.39S07.003 DY
GND1 SPRING-62-GP 34.39S07.003 DY

MXM

S1 SPRING-37-GP-U 34.15F09.001 DY
S2 SPRING-37-GP-U 34.15F09.001 DY
S3 SPRING-37-GP-U 34.15F09.001 DY

SPRING ON TOP

SD_0903

Touch Pad

H30 SPRING-57-GP 34.42T14.002

HDMI

SW2 SPRING-15-GP DY

SB-U15

SW3 SPRING-7 DY
SW4 SPRING-7 DY
SW5 SPRING-7 DY

USB

SW6 SPRING-6 DY
SW7 SPRING-6 DY

Jack

SW8 SPRING-15-GP DY

RN24

SW9 SPRING-7 DY

Check test point

3D3V_S0		TP263 TPAD14-GP
3D3V_AUX_S5		TP226 TPAD14-GP
3D3V_S5		TP262 TPAD14-GP
5V_S5		TP246 TPAD14-GP
21,41	PM_PWRBTN#	TP253 TPAD14-GP
6,20	CPU_PWRGD	TP141 TPAD14-GP
25,41	S5_ENABLE	TP143 TPAD14-GP
6,20	CPU_LDT_RST#	TP238 TPAD14-GP

Test Point放在Dimm Door打開可量測處

STAND OFF ON BOTTOM

CPU & NB

H31 HOLE 34.42Y01.011
H32 HOLE 34.42Y01.011
H33 HOLE 34.42Y01.011
H34 HOLE 34.42Y01.011

Mini Card

H19 HOLE 34.4Z402.001
H20 HOLE 34.4Z402.001

MXM

H14 HOLE DIS 34.4Z401.001
H17 HOLE DIS 34.4Z401.001

STAND OFF ON TOP

MDC

H21 HOLE 34.42Y01.011
H22 HOLE 34.42Y01.011

H1 PAD-1P-3-GP
H2 PAD-1P-3-GP
H3 PAD-1P-3-GP
H4 PAD-1P-3-GP
H5 PAD-1P-3-GP
H6 PAD-1P-3-GP
H7 PAD-1P-3-GP
H8 PAD-1P-3-GP
H9 PAD-1P-3-GP
H10 PAD-1P-3-GP
H13 PAD-1P-3-GP
H18 PAD-1P-3-GP
PAD1 PAD-1P-4-GP
H39 PAD-1P-3-GP
H40 PAD-1P-3-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size: A3 | Document Number: Big Bear 2A | Rev: SD

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REAR1

39,40	SPKR_L-	TP1	AFTE14P-GP
39,40	SPKR_L+	TP2	AFTE14P-GP
39,40	SPKR_R-	TP3	AFTE14P-GP
39,40	SPKR_R+	TP4	AFTE14P-GP

FRONT1

39,40	CEN+	TP162	AFTE14P-GP
39,40	CEN-	TP163	AFTE14P-GP

INT. MIC

38,40	INT_MIC1_CN	TP5	AFTE14P-GP

EKCN1

	3D3V_AUX_S5	TP57	AFTE14P-GP
15	LID_CLOSE#_R	TP60	AFTE14P-GP
15	E-BUTTON#_R	TP47	AFTE14P-GP

LEDB1

	3D3V_AUX_S5	TP55	AFTE14P-GP
	5V_S0	TP56	AFTE14P-GP
15	BAT_SCL_R	TP179	AFTE14P-GP
15	I2C_INT_R	TP173	AFTE14P-GP
15	BAT_SDA_R	TP177	AFTE14P-GP

KB1

41	KROW8	TP96	AFTE14P-GP
41	KROW6	TP103	AFTE14P-GP
41	KROW7	TP83	AFTE14P-GP
41	KROW5	TP84	AFTE14P-GP
41	KROW4	TP104	AFTE14P-GP
41	KROW3	TP85	AFTE14P-GP
41	KROW2	TP97	AFTE14P-GP
41	KROW1	TP86	AFTE14P-GP
41	KCOL18	TP98	AFTE14P-GP
41	KCOL17	TP87	AFTE14P-GP
41	KCOL16	TP105	AFTE14P-GP
41	KCOL15	TP93	AFTE14P-GP
41	KCOL14	TP106	AFTE14P-GP
41	KCOL13	TP94	AFTE14P-GP
41	KCOL12	TP107	AFTE14P-GP
41	KCOL11	TP95	AFTE14P-GP
41	KCOL10	TP108	AFTE14P-GP
41	KCOL9	TP88	AFTE14P-GP
41	KCOL8	TP99	AFTE14P-GP
41	KCOL7	TP89	AFTE14P-GP
41	KCOL6	TP100	AFTE14P-GP
41	KCOL5	TP90	AFTE14P-GP
41	KCOL4	TP101	AFTE14P-GP
41	KCOL3	TP91	AFTE14P-GP
41	KCOL2	TP102	AFTE14P-GP
41	KCOL1	TP92	AFTE14P-GP

PWCN1

	5V_S0	TP31	AFTE14P-GP
	5V_S5	TP49	AFTE14P-GP
17	L-line_LED#_R	TP66	AFTE14P-GP
17	NUM_LED#_R	TP53	AFTE14P-GP
17	MEDIA_LED#_R	TP30	AFTE14P-GP
17	CAP_LED#_R	TP35	AFTE14P-GP
17	KBC_PWRBTN#_R	TP38	AFTE14P-GP
17	FRONT_PWRLED#_1	TP39	AFTE14P-GP
17	STDBY_LED#_1	TP266	AFTE14P-GP

FP2

	3D3V_S0	TP46	AFTE14P-GP
21,31	USBPP6	TP34	AFTE14P-GP
21,31	USBPN6	TP41	AFTE14P-GP
31,41	FP_DETECT#	TP32	AFTE14P-GP
21,31	FP_ID	TP42	AFTE14P-GP
31,41	TP_LEFT	TP33	AFTE14P-GP
31,41	TP_RIGHT	TP40	AFTE14P-GP

TPDA1

	5V_S0	TP44	AFTE14P-GP
41	TP_DATA	TP37	AFTE14P-GP
41	TP_CLK	TP43	AFTE14P-GP
31,41	TP_RIGHT	TP36	AFTE14P-GP
31,41	TP_LEFT	TP45	AFTE14P-GP

BLUE1

21,28	USBPP5	TP159	AFTE14P-GP
21,28	USBPN5	TP160	AFTE14P-GP
	3D3V_BT_S0	TP158	AFTE14P-GP

USBCN1

	5V_S5	TP161	AFTE14P-GP
	5V_S5	TP164	AFTE14P-GP
21,30	USB_OC#4	TP166	AFTE14P-GP
30,41	USB_PWR_EN#	TP165	AFTE14P-GP
21,30	USBPN4	TP168	AFTE14P-GP
21,30	USBPP4	TP167	AFTE14P-GP
21,30	USBPN8	TP171	AFTE14P-GP
21,30	USBPP8	TP170	AFTE14P-GP

FAN1

25	FAN1_FG1	TP25	AFTE14P-GP
	FAN1_VCC	TP26	AFTE14P-GP

BAT1

52	BATA_SDA_1	TP9	AFTE14P-GP
52	BATA_SCL_1	TP8	AFTE14P-GP
	BT+	TP11	AFTE14P-GP
	BT+	TP10	AFTE14P-GP
	BT+	TP14	AFTE14P-GP
51,52	BATT_SENSE	TP13	AFTE14P-GP
52	BAT_IN#_CN	TP7	AFTE14P-GP

DC1

	AD_JK	TP12	AFTE14P-GP
	AD_JK	TP16	AFTE14P-GP
	AD_JK	TP15	AFTE14P-GP

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size: A3 | Document Number: **Big Bear 2A** | Rev: SC

Date: Monday, October 27, 2008 | Sheet 54 of 57